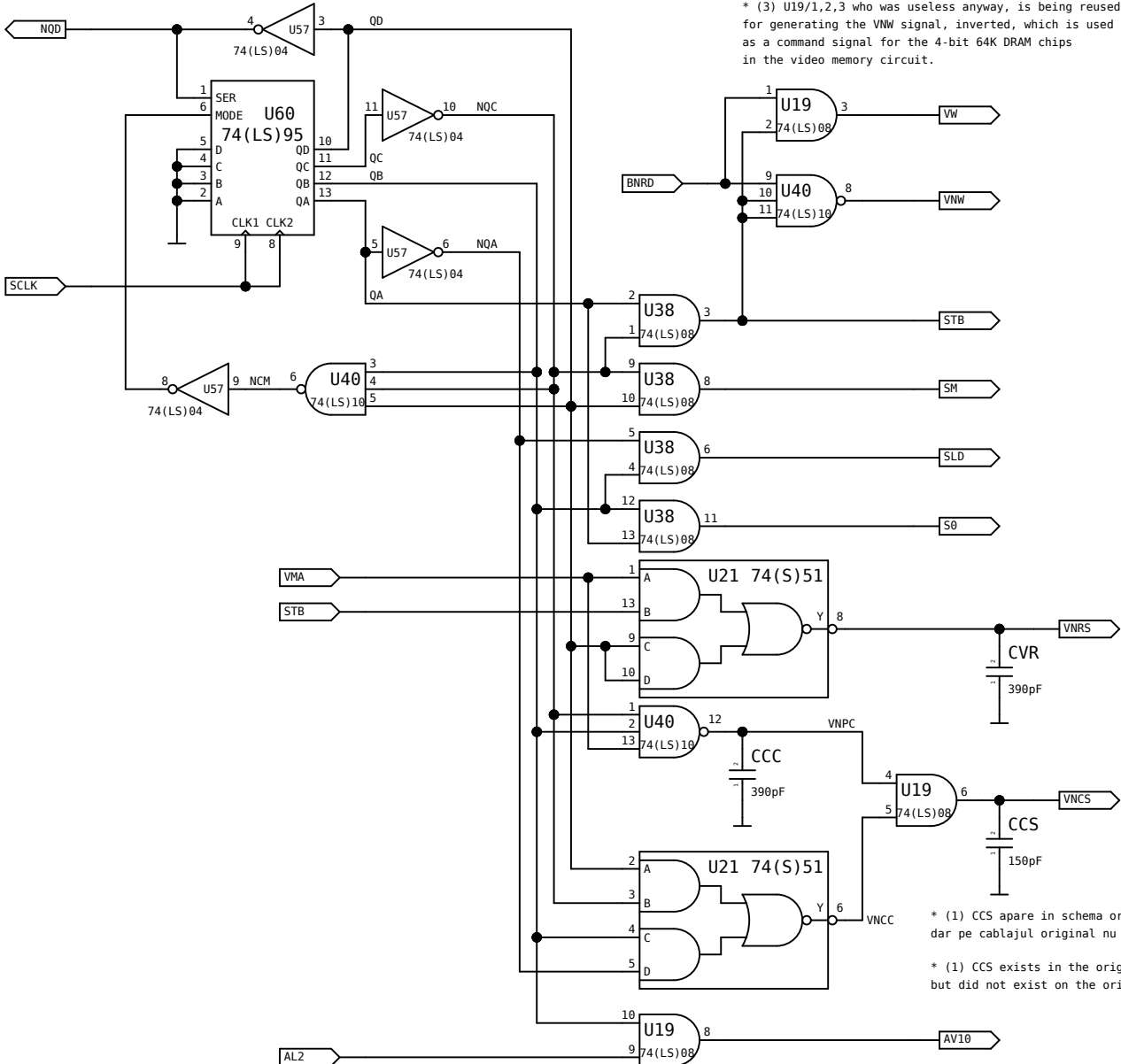


* (3) U19/1,2,3 care era oricum inutil, este reutilizat in scopul obtinerii semnalului VNW inversat, pentru comanda memoriilor DRAM pe 4 biti din circuitul memoriei video.

* (3) U19/1,2,3 who was useless anyway, is being reused for generating the VNW signal, inverted, which is used as a command signal for the 4-bit 64K DRAM chips in the video memory circuit.

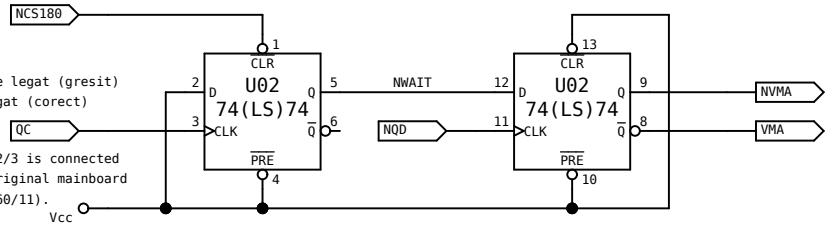


* (1) CCS apare in schema originala, dar pe cablajul original nu era prevazut

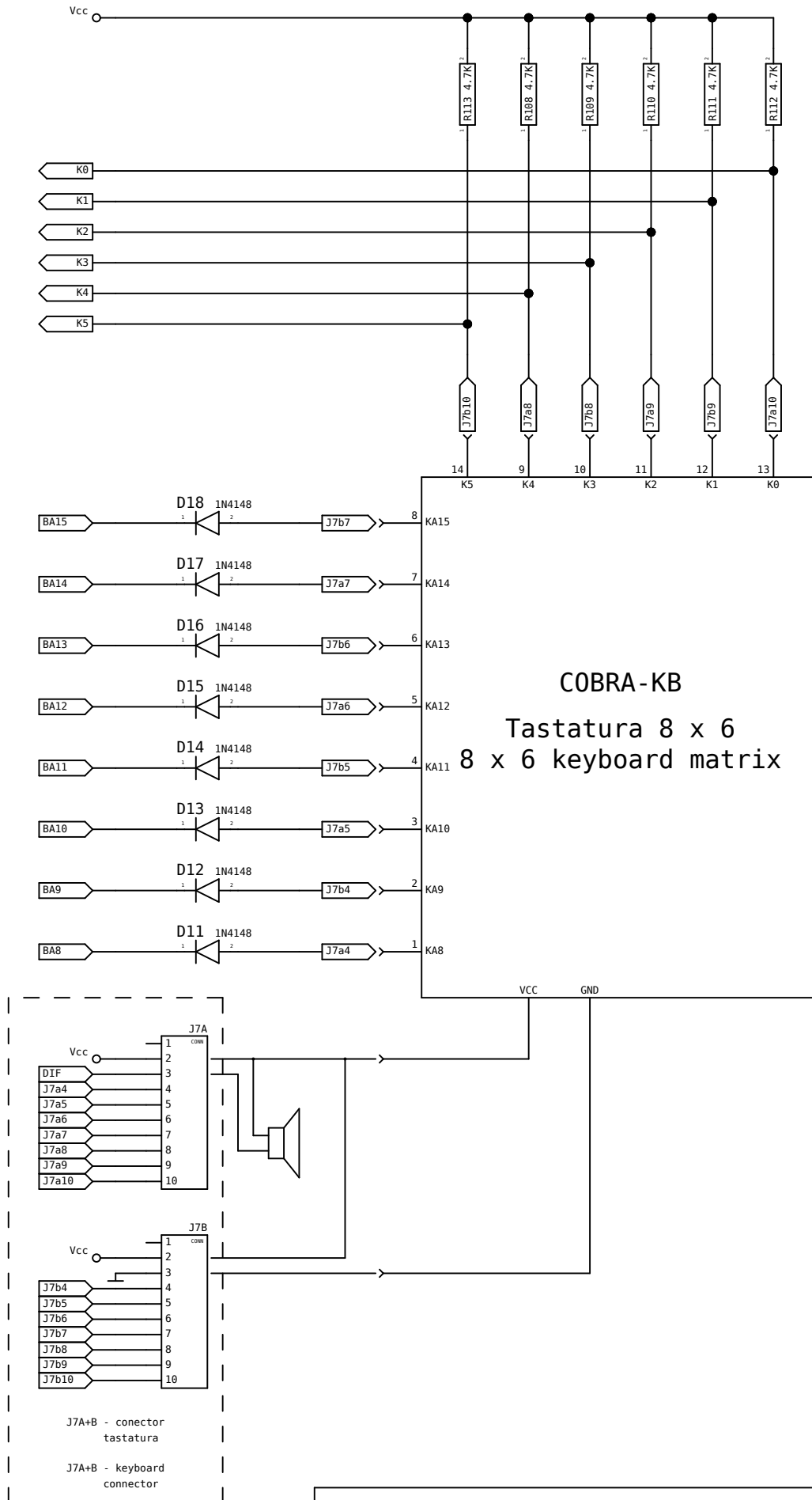
* (1) CCS exists in the original schematics, but did not exist on the original mainboard.

* (2) In schema originala, U02/3 este legat (gresit) la QD (U60/10) dar pe cablaj este legat (corect) la QC (U60/11)

* (2) In the original schematics, U02/3 is connected (wrong) to QD (U60/10), but on the original mainboard it is connected (correctly) to QC (U60/11).



TITLE		µC CoBra - Arbitrul de memorie si logica de comanda	
		CoBra µC - Memory access prioritizer and command logic	
FILE:	CoBra	REVISION:	4.24 (DRAM upgrade, 64KB DRAM)
PAGE	1 OF 19	DRAWN BY:	ElectroNnix



TITLE μ C CoBra - Circuitul de conectare tastatura
CoBra μ C - Keyboard interfacing circuit

FILE: CoBra

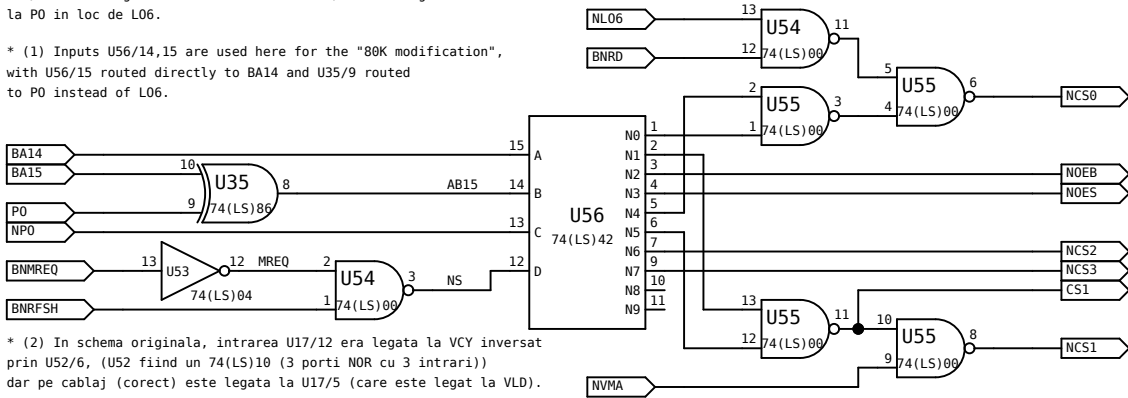
REVISION: 3 (original design, 64KB DRAM)

PAGE 2 OF 19

DRAWN BY: ElectronNix

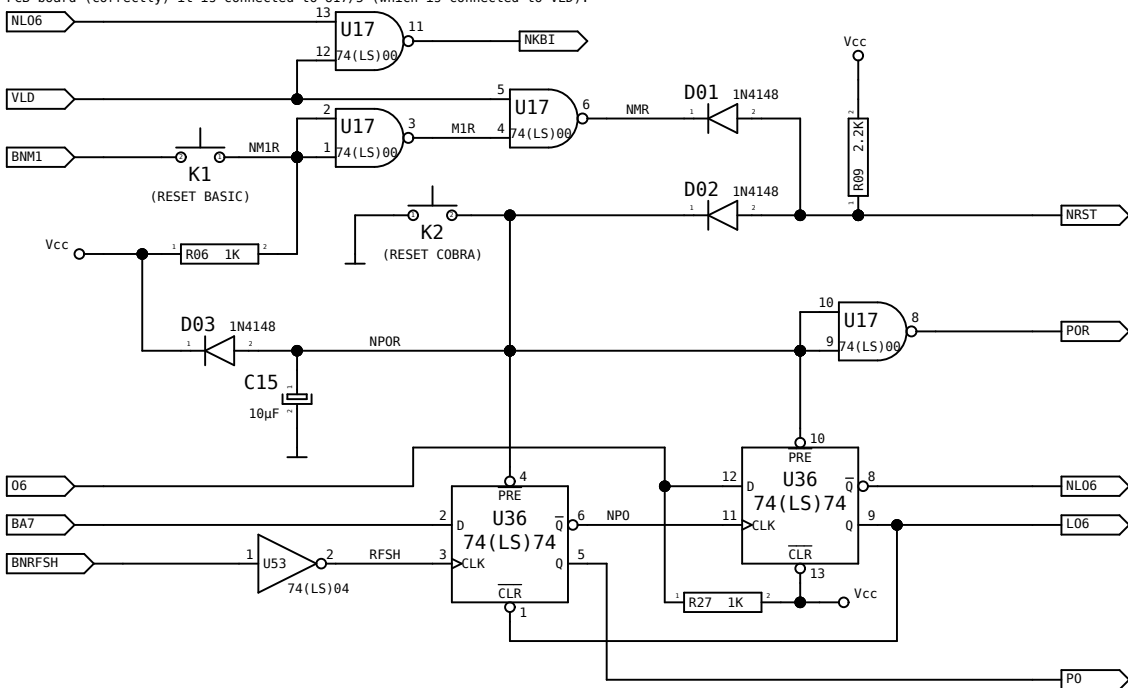
* (1) Intrarile U56/14,15 sint folosite aici pentru "modificarea de 80K", U56/15 fiind legata direct la BA14 iar U35/9 fiind legata la P0 in loc de L06.

* (1) Inputs U56/14,15 are used here for the "80K modification", with U56/15 routed directly to BA14 and U35/9 routed to P0 instead of L06.



* (2) In schema originala, intrarea U17/12 era legata la VCY inversat prin U52/6, (U52 fiind un 74(LS)10 (3 porti NOR cu 3 intrari)) dar pe cablaj (corect) este legata la U17/5 (care este legat la VLD).

* (2) In the original schematics, input U17/12 was connected to VCY inverted through U52/6, (U52 being a 74(LS)10 (3 NOR 3-input gates)) but on the PCB board (correctly) it is connected to U17/5 (which is connected to VLD).



TITLE μ C CoBra - Circuitul de configurare si selectie
CoBra μ C - Configurator and selector circuit

FILE: CoBra

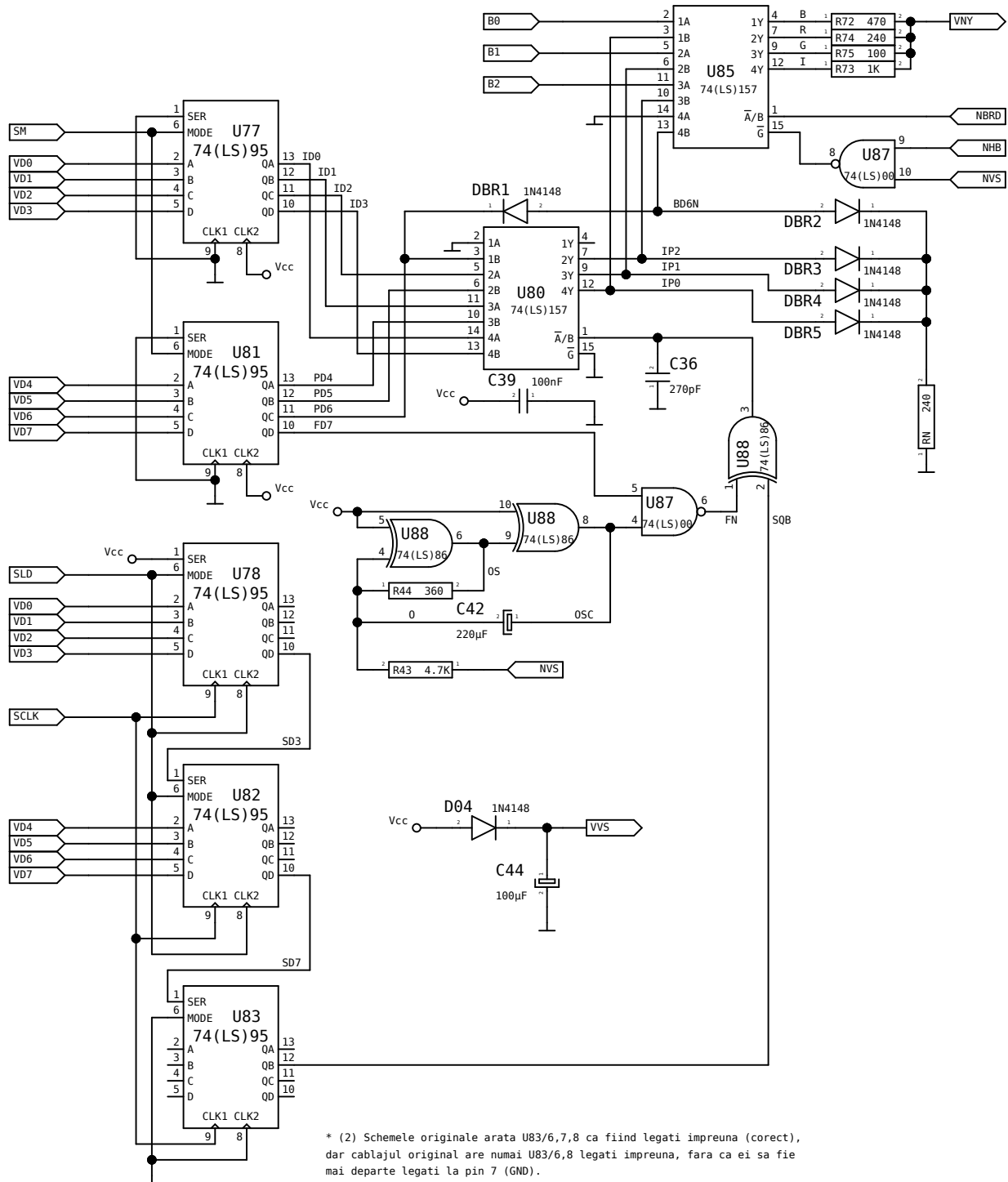
REVISION: 4.3 (80KB DRAM)

PAGE 3 OF 19

DRAWN BY: ElectronNix

* (1) In schema originala, diodele DBR1-5 si rezistenta RN sint desenate (cu toate ca diodele nu sint denumite) dar pe cablajul original nu sint prevazute, iar U85/13 este legat direct la U80/3. Ca urmare, cablajul original nu permitea functia de BRIGHT. Am modificat cablajul adaugand gauri pentru BDR1-5 si RN si intrerupind deci legatura directa dintre U85/13 si U80/3.

* (1) In the original schematics, diodes DBR1-5 and resistor RN are drawn (although the diodes don't have names) but on the original mainboard they are not placed, and U85/13 is directly connected to U80/3. Therefore, the original mainboard would not allow the BRIGHT function. I have modified the mainboard layout by adding mounting holes for BDR1-5 and RN and therefore interrupting the direct connection between U85/13 and U80/3.



* (2) Schemele originale arata U83/6,7,8 ca fiind legati impreuna (corect), dar cablajul original are numai U83/6,8 legati impreuna, fara ca ei sa fie mai departe legati la pin 7 (GND). Am modificat cablajul placii de baza pentru a corespunde schemei originale. (Vezi legatura #25 fata 2)

* (2) The original schematics show U83/6,7,8 connected together (correctly), but the original mainboard layout only has U83/6,8 connected together without them being further connected to pin 7 (GND). I have modified the mainboard layout to match the original schematics. (See rewiring #25 side 2)

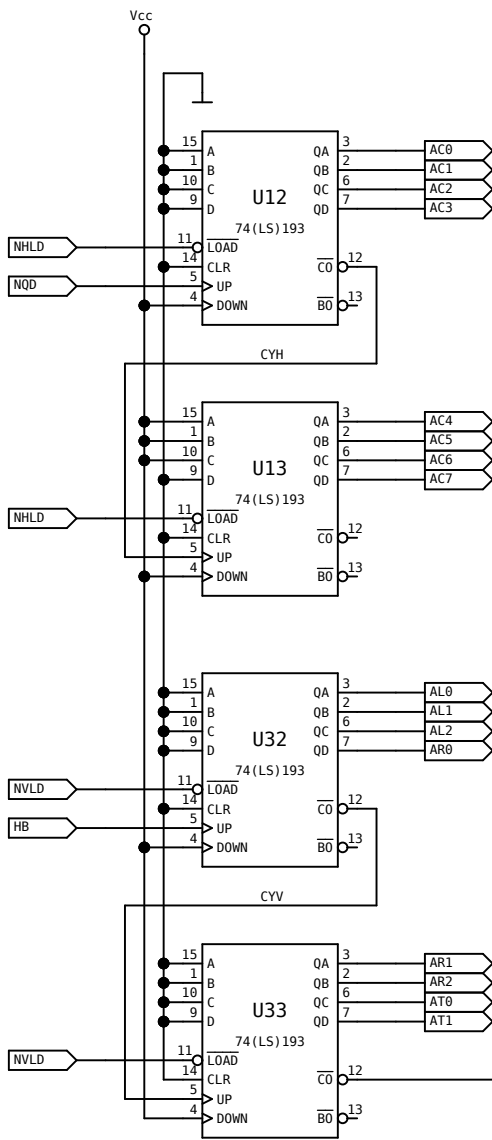
TITLE μ C CoBra - Circuitul formator semnal video
CoBra μ C - Video signal generator circuit

FILE: CoBra

REVISION: 3 (original design, 64KB DRAM)

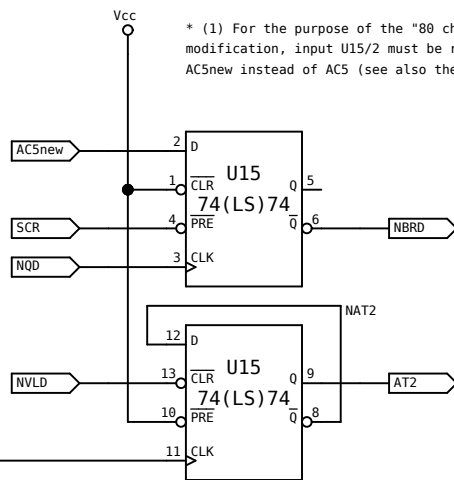
PAGE 4 OF 19

DRAWN BY: ElectroNnix



* (1) Pentru realizarea modificarii de 80 caractere pe linie in CP/M, intrarea U15/2 va primi semnalul AC5new in loc de AC5 (vezi pagina cu "Modificari")

* (1) For the purpose of the "80 char/line in CPM" modification, input U15/2 must be routed to signal AC5new instead of AC5 (see also the "Modifications" page)



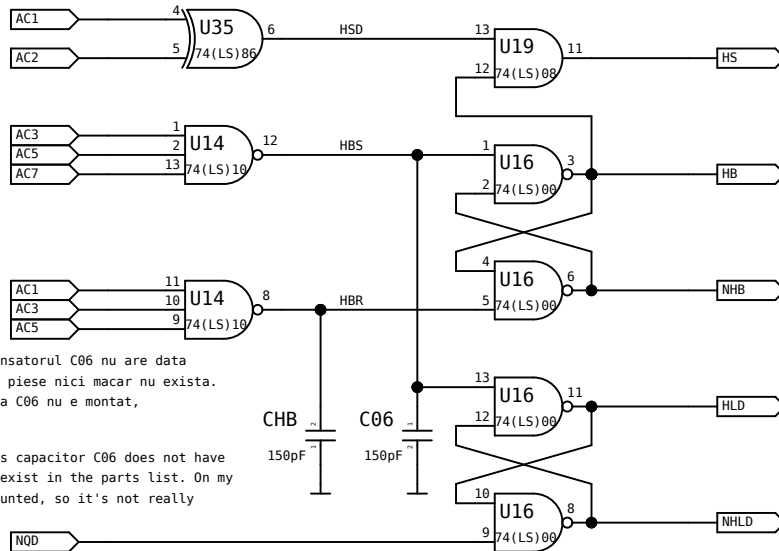
TITLE μ C CoBra - Circuitul de generare adrese video
CoBra μ C - Video address generator circuit

FILE: CoBra

REVISION: 4.3 (80KB DRAM)

PAGE 5 OF 19

DRAWN BY: ElectronNix

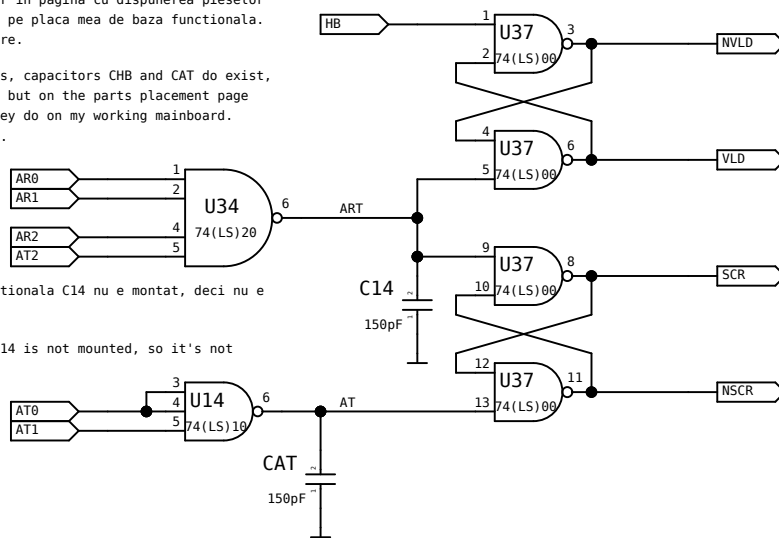


* (1) In schema originala condensatorul C06 nu are data nici o valoare, iar in lista de piese nici macar nu exista. Pe placa mea de baza functionala C06 nu e montat, deci nu e intr-adevar necesar.

* (1) In the original schematics capacitor C06 does not have any value, and it doesn't even exist in the parts list. On my working mainboard C06 is not mounted, so it's not really required.

* (2) In schema originala condensatoarele CHB si CAT exista, exista si in lista de piese, dar in pagina cu dispunerea pieselor ele nu exista si nu exista nici pe placa mea de baza functionala. Deci nu sint intr-adevar necesare.

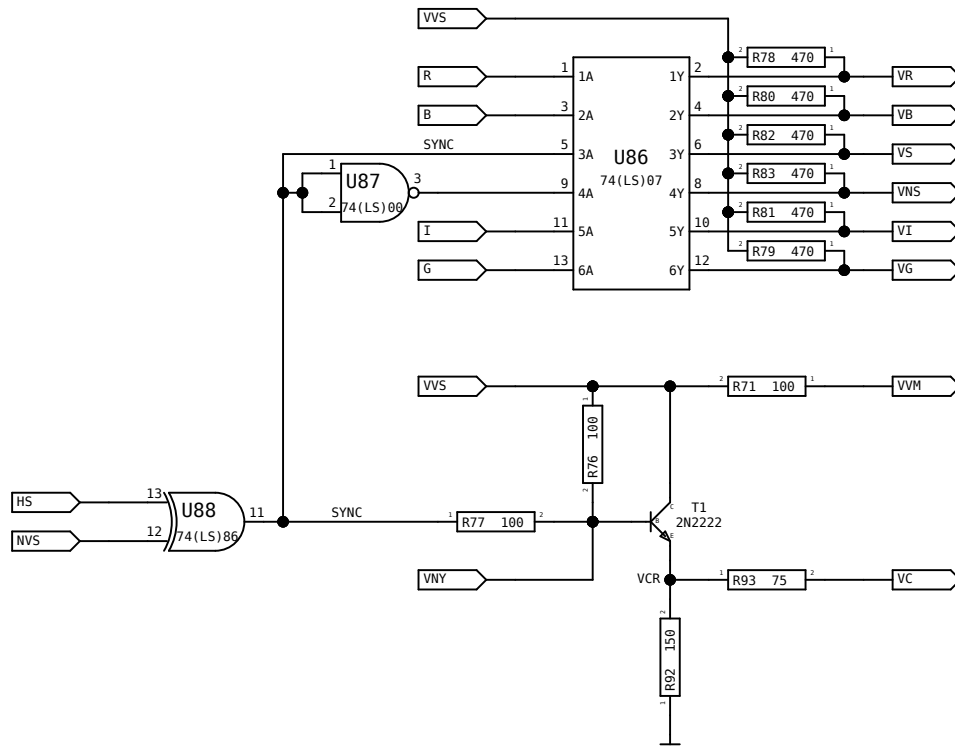
* (2) In the original schematics, capacitors CHB and CAT do exist, they also do in the parts list, but on the parts placement page they don't exist and neither they do on my working mainboard. So they are not really required.



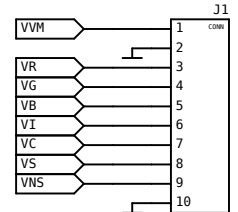
* (3) Pe placa mea de baza functionala C14 nu e montat, deci nu e intr-adevar necesar.

* (3) On my working mainboard C14 is not mounted, so it's not really required.

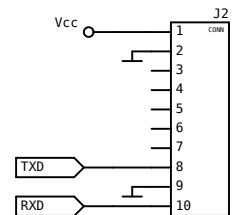
TITLE		μC CoBra - Circuitul generator de sincroimpulsuri CoBra μC - Video sync pulses generator circuit	
FILE:	CoBra	REVISION:	3 (original design, 64KB DRAM)
PAGE	6 OF 19	DRAWN BY:	ElectroNNix



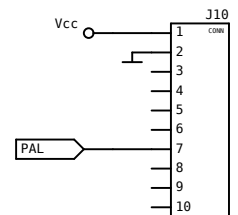
J1 - CONECTOR VIDEO
J1 - VIDEO CONNECTOR



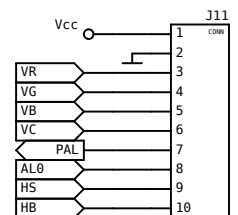
J2 - CONECTOR RS232
J2 - RS232 CONNECTOR



J10 - CONECTOR PAL VIDEO
J10 - PAL VIDEO CONNECTOR



J11 - CONECTOR CODOR PAL
J11 - PAL CODER CONNECTOR



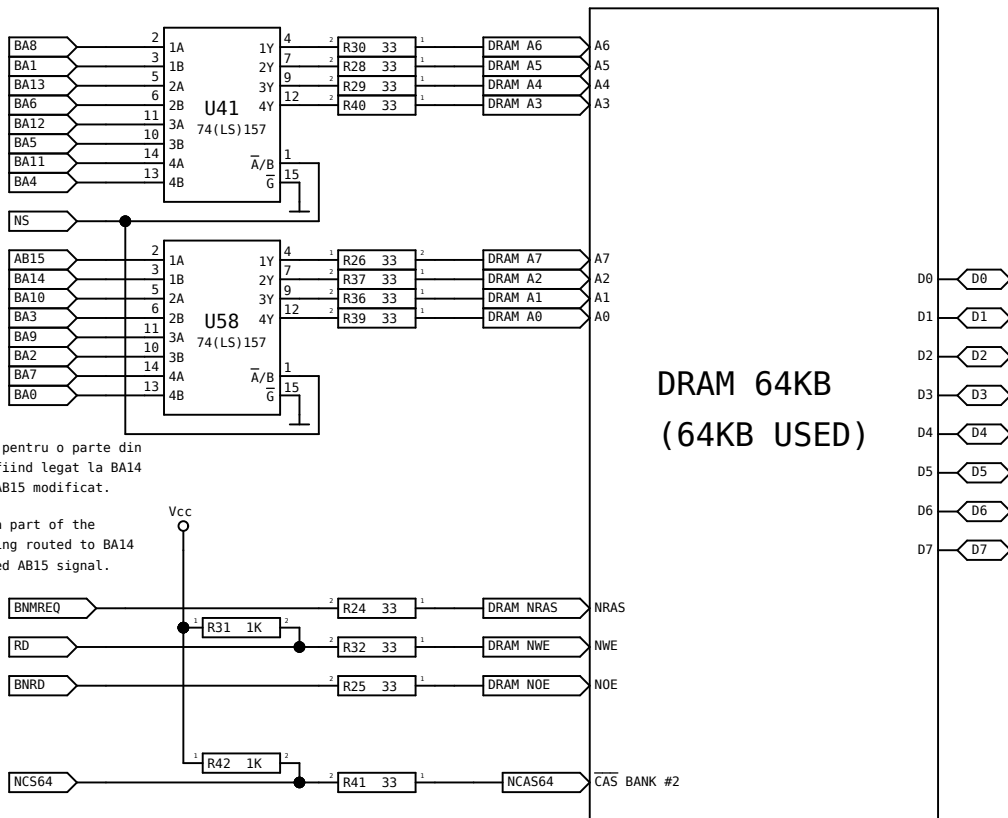
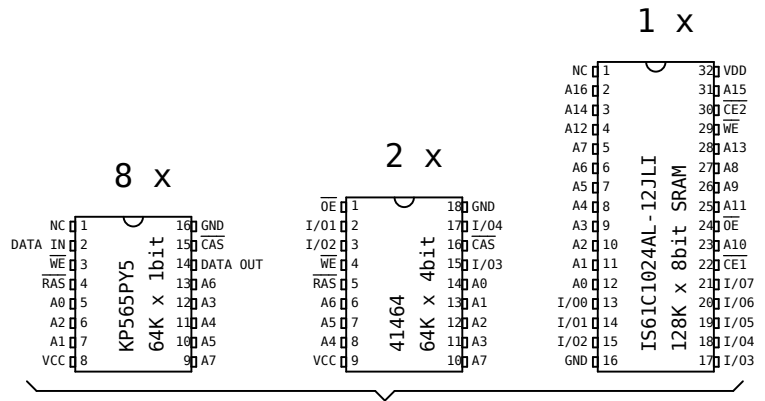
TITLE μ C CoBra - Circuitul de interfata cu monitorul TV
CoBra μ C - TV monitor interfacing circuit

FILE: CoBra

REVISION: 4.21 ROM upgrade, 64KB DRAM)

PAGE 7 OF 19

DRAWN BY: ElectroNnix



* (1) U58/2,3,4 este folosit pentru o parte din "modificarea de 80K", U58/3 fiind legat la BA14 iar U58/2 primind un semnal AB15 modificat.

* (1) U58/2,3,4 is used for a part of the "80K modification", U58/3 being routed to BA14 and U58/2 receiving a modified AB15 signal.

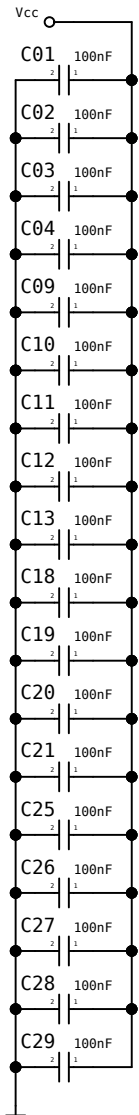
TITLE μ C CoBra - Circuitul memoriei dinamice - pag.1/2
CoBra μ C - Dynamic memory circuit - pag.1/2

FILE: CoBra

REVISION: 4.3 (80KB DRAM)

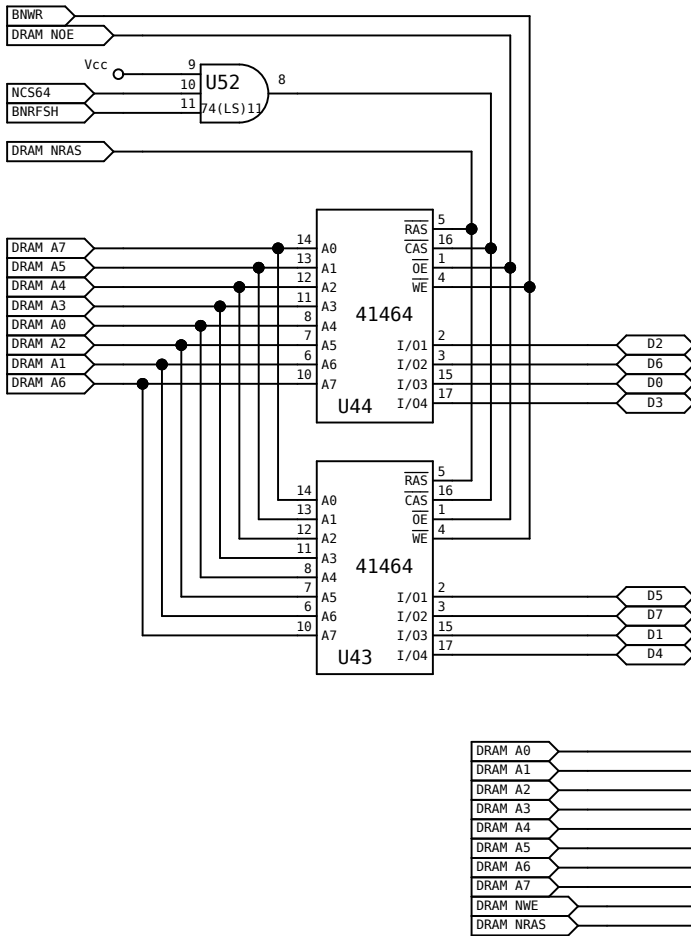
PAGE 8 OF 19

DRAWN BY: ElectronNix

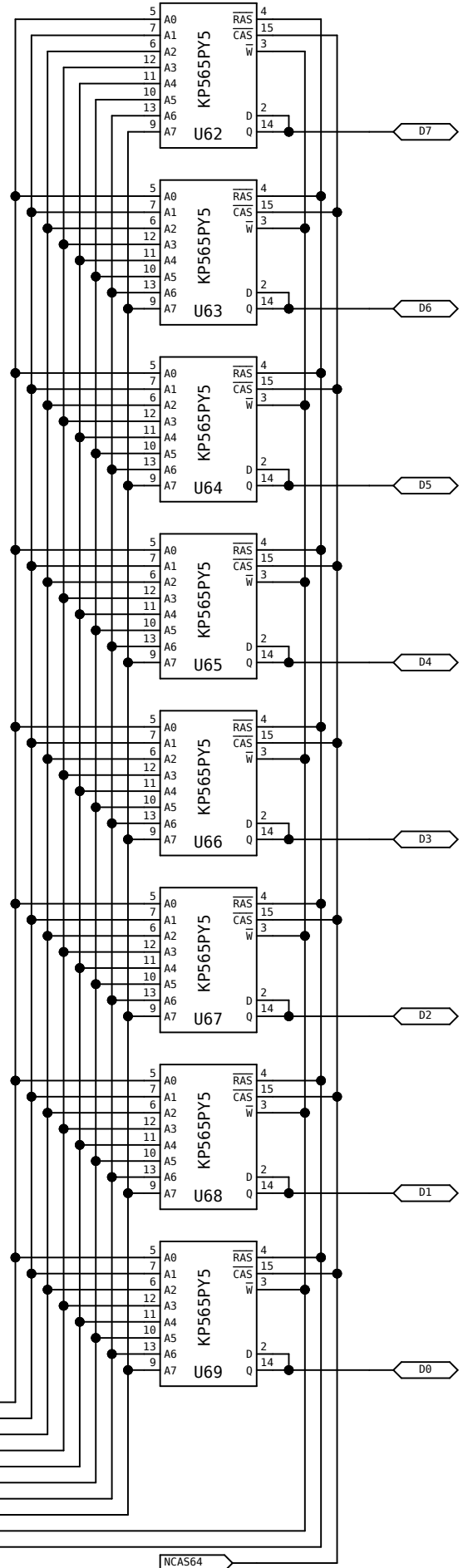


* (1) Poarta U52/8,9,10,11 furnizeaza un refresh de tip "CAS before RAS" pentru cele doua cipuri de memorie dinamica 41464, pentru a evita necesitatea celui de-al optulea bit de adresa (A7) pentru refresh-ul "RAS Only", in conditiile in care Z80 foloseste doar 7 linii de adresa (A0-A6) la executia refresh-ului, iar memoriile 41464 necesita 8 linii de adresa (A0-A7) daca refresh-ul folosit este de tip "RAS Only".

* (1) Gate U52/8,9,10,11 provides a "CAS before RAS" refresh to the two 41464 dynamic memories, in order to avoid the necessity of the 8th address bit (A7) for the "RAS Only" refresh, since Z80 only uses 7 address lines (A0-A6) for refresh and the 41464 dynamic memories require 8 address lines (A0-A7) if the refresh being applied is of "RAS Only" type.



DRAM #2



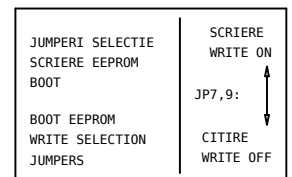
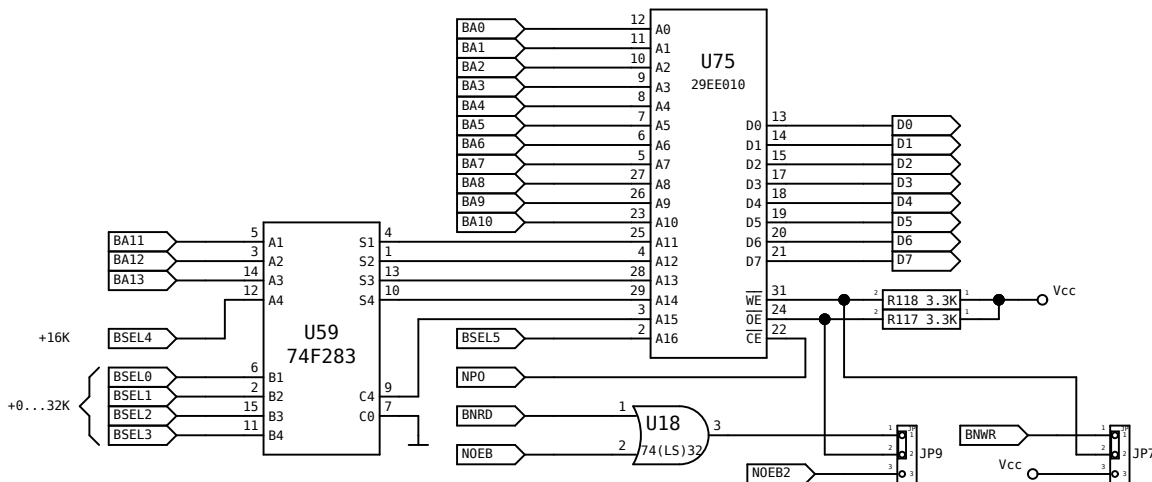
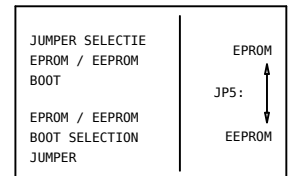
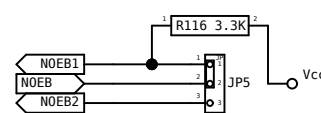
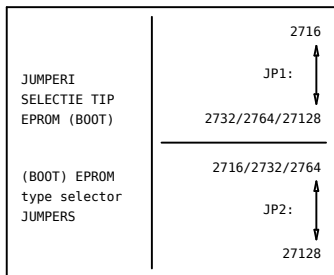
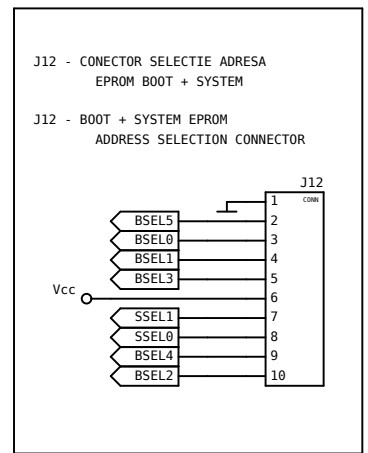
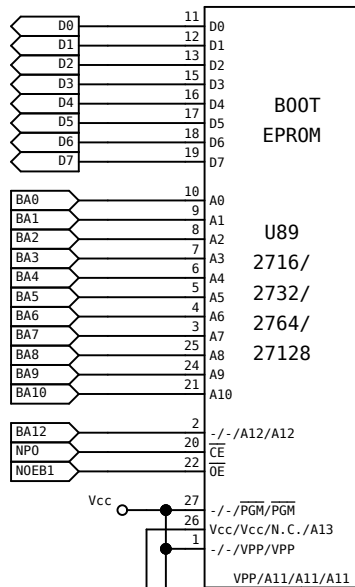
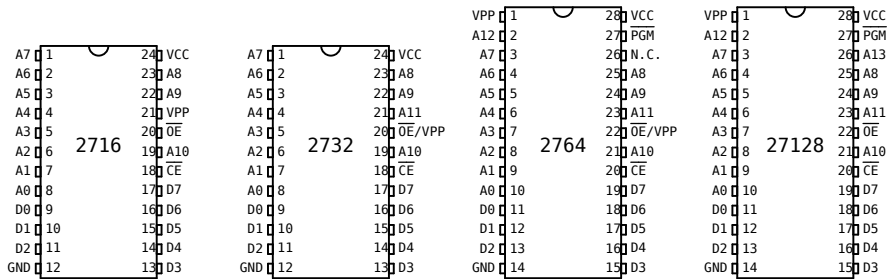
TITLE μ C CoBra - Circuitul memoriei dinamice - pag.2/2
CoBra μ C - Dynamic memory circuit - pag.2/2

FILE: CoBra

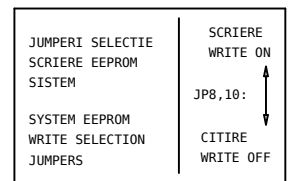
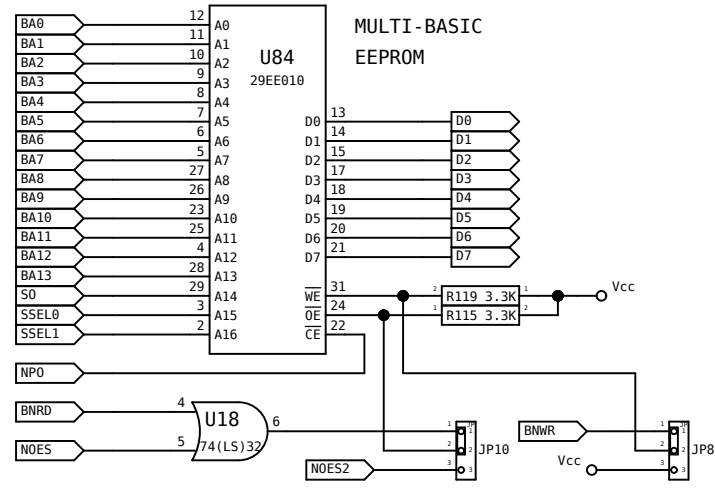
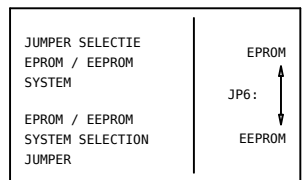
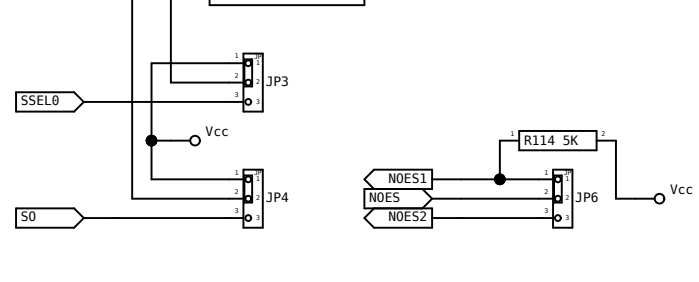
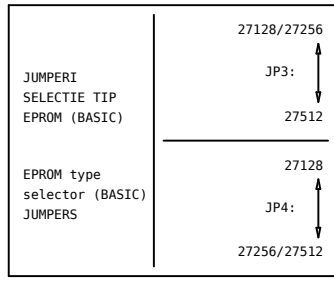
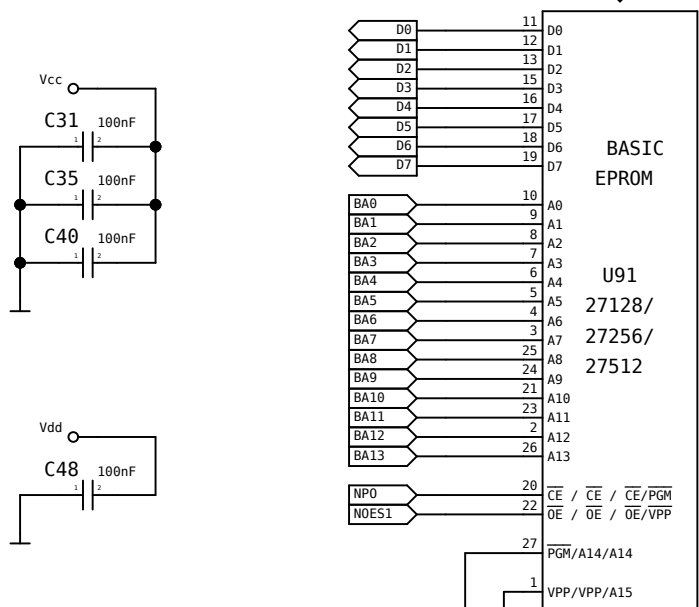
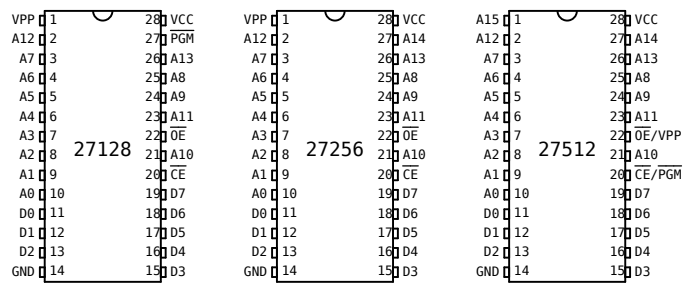
REVISION: 4.24 (DRAM upgrade, 64KB DRAM)

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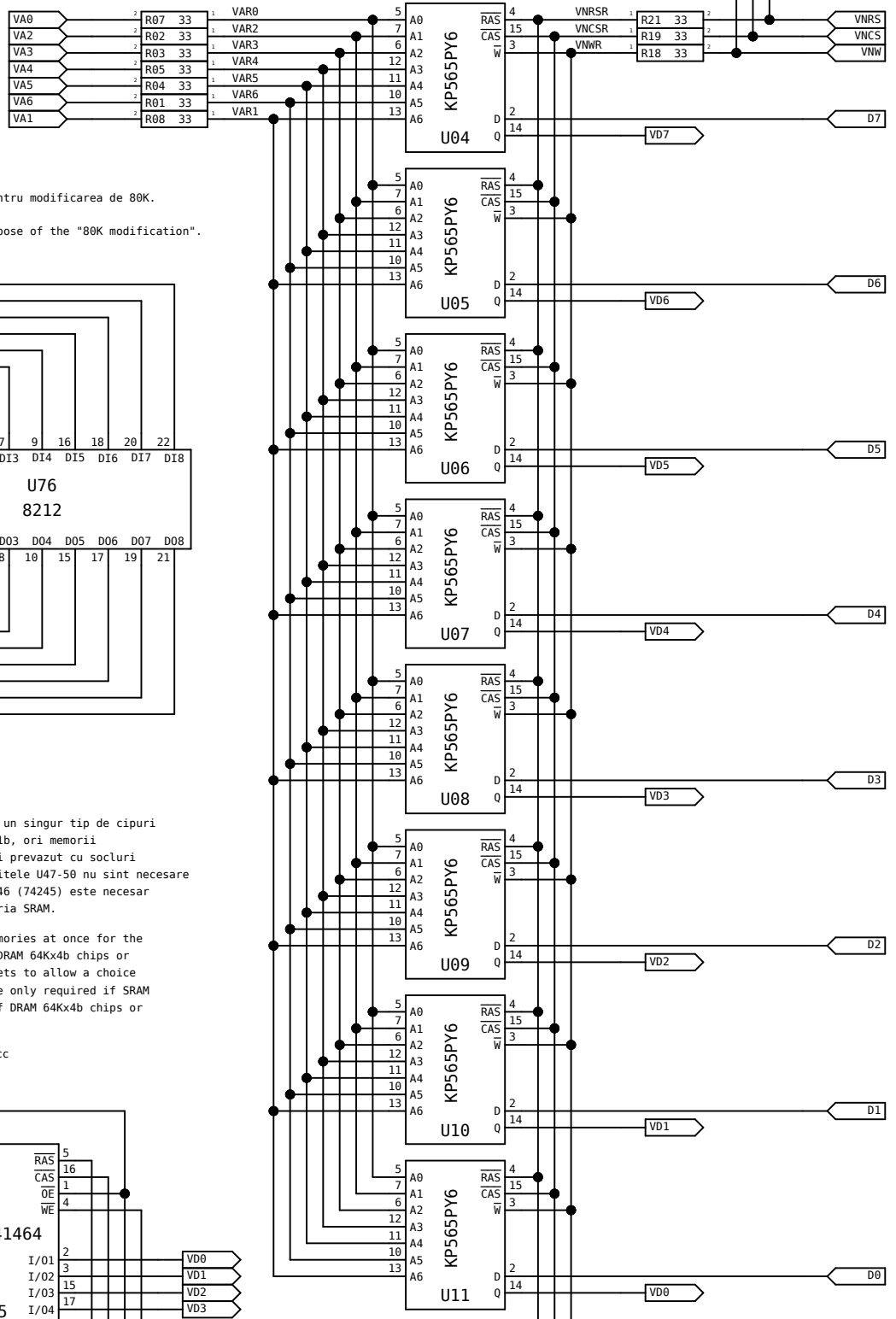
DRAWN BY: ElectronNix



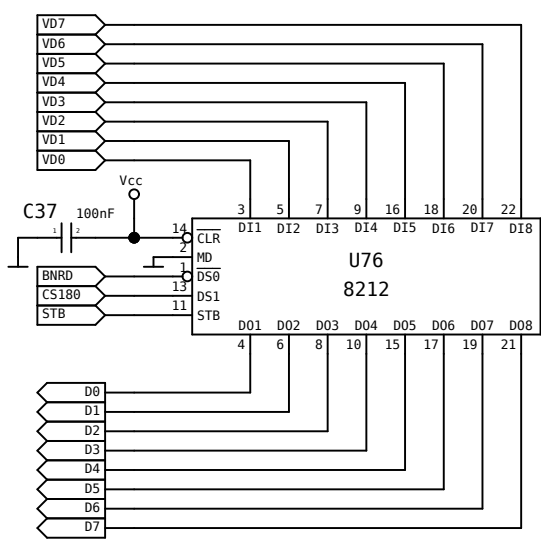
TITLE μ C CoBra - Circuitul memoriei nevolatile - pag.1/2		CoBra μ C - Read-only memory circuit - pag.1/2	
FILE:	CoBra	REVISION:	4.21 (ROM upgrade, 64KB DRAM)
PAGE	10 OF 19	DRAWN BY:	ElectroNNix



TITLE		µC CoBra - Circuitul memoriei nevolatile - pag.2/2	
		CoBra µC - Read-only memory circuit - pag.2/2	
FILE:	CoBra	REVISION:	4.21 (ROM upgrade, 64KB DRAM)
PAGE	11 OF 19	DRAWN BY:	ElectroNNix

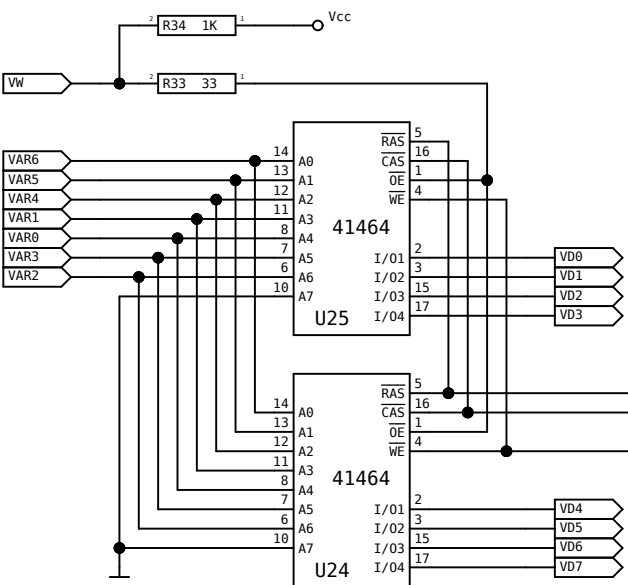


* (2) Intrarea U76/13 este folosita aici pentru modificarea de 80K.
 * (2) Input U76/13 is used here for the purpose of the "80K modification".



* (1) La un moment dat se poate folosi doar un singur tip de cipuri pentru memoria video: ori memorii DRAM 16Kx1b, ori memorii DRAM 64Kx4b ori memoria SRAM. Cablajul va fi prevazut cu socluri pentru a putea alege varianta dorita. Circuitetele U47-50 nu sint necesare decit daca se foloseste memoria SRAM, iar U46 (74245) este necesar doar daca se foloseste DRAM 64Kx4b sau memoria SRAM.

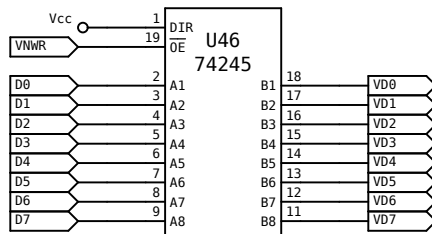
* (1) There can only be used one type of memories at once for the video memory: either DRAM 16Kx1b chips, or DRAM 64Kx4b chips or one SRAM chip. The mainboard will have sockets to allow a choice between these 3 options. Circuits U47-50 are only required if SRAM is used, and U46 (74245) is only required if DRAM 64Kx4b chips or SRAM is used.



* (2) Memoriile 41464 sint aici folosite la un sfert din capacitate, adica 16KB. Memoriile echivalente de 16K x 4b, adica 4416, au acelasi numar de pini dar multiplexarea adreselor este diferita, asa ca am hotarit sa folosesc 41464 care la ora actuala se gasesc si la un pret mai mic.

* (2) 41464 are used at 1/4 capacity here, that is 16KB. The equivalent 16K x 4b chips, that is 4416, have the same number of pins but address multiplexing is different, so I decided I will use 41464 which currently are available for a smaller price.

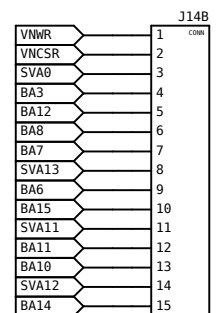
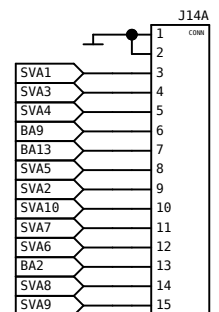
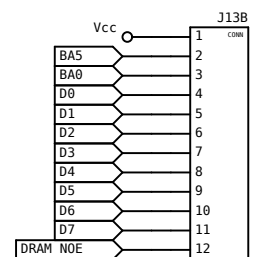
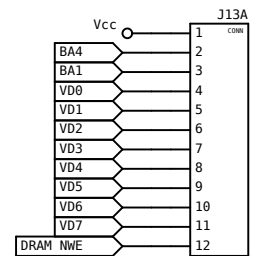
TITLE		µC CoBra - Circuitul memoriei video - pag.1/2	
		CoBra µC - Video memory circuit - pag.1/2	
FILE:	CoBra	REVISION:	4.3 (80KB DRAM)
PAGE	12 OF 19	DRAWN BY:	ElectroNNix



* (2) 74245 are rolul de a conecta magistrala de date la magistrala de date video numai pe durata scrierii de date dinspre procesor in memoria video. In restul timpului liniile de date D0-D7 sint izolate de liniile de date video VD0-VD7. Acest lucru este necesar pentru memoriile DRAM 41464 si pentru memoria RAM statica 61C256, intrucit aceste cipuri nu mai au datele de intrare separate de datele de iesire.

* (2) 74245 has the purpose of connecting the data bus to the video data bus only while the processor writes data to the video memory. In the rest of the time the data lines D0-D7 are disconnected from the video data lines VD0-VD7. This is required for the 41464 DRAM chips and the 61C256 static RAM chip since they do not have data inputs separated from the data outputs.

J13A+B, J14A+B
Conectori modul SRAM
SRAM module connectors



TITLE μ C CoBra - Circuitul memoriei video - pag.2/2
CoBra μ C - Video memory circuit - pag.2/2

FILE: CoBra

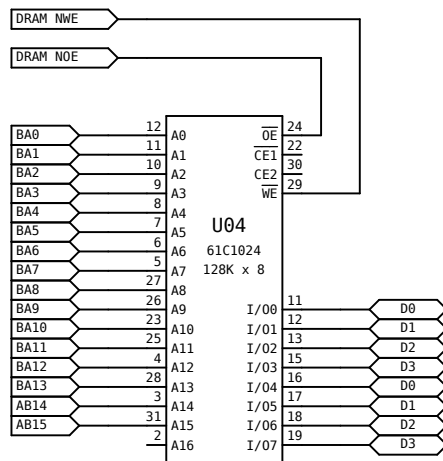
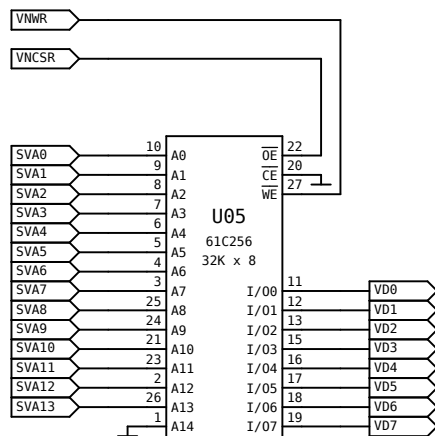
REVISION: 4.24 (DRAM upgrade, 64KB DRAM)

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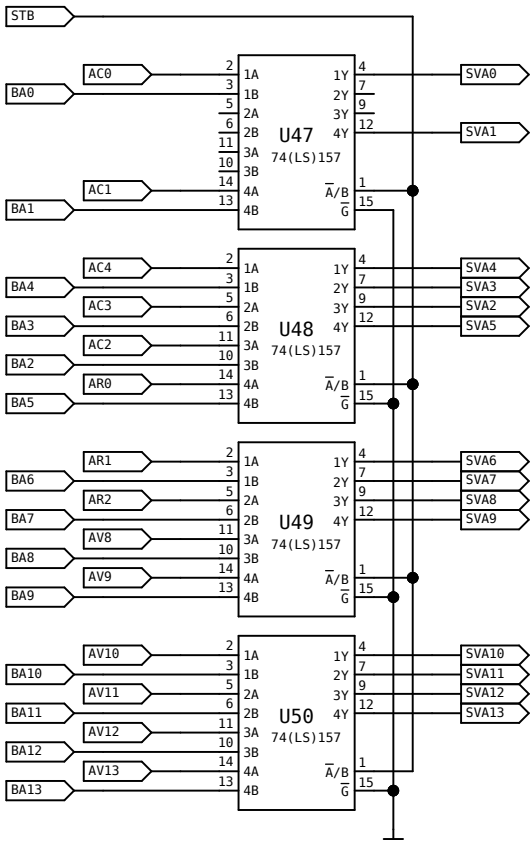
DRAWN BY: ElectroNnix

* (1) Memoria statica 61C256 este aici folosita la jumatate de capacitate (16KB).
 Am folosit acest tip de memorie din doua motive: perspectiva unei eventuale
 extensii de memorie si faptul ca memorii mai mici nu am gasit la furnizori.

* (1) The static DRAM chip 61C256 is used here at half its capacity (16KB).
 I have chosen this particular chip for two reasons: the perspective of a
 possible memory extension and the lack of a 16KB chip from suppliers.

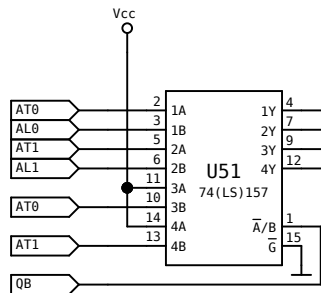


TITLE μC CoBra - Circuitul modulului memoriei statice CoBra μC - Static memory module circuit	
FILE: CoBra	REVISION: 4.24 (DRAM upgrade, 64KB DRAM)
PAGE 14 OF 19	DRAWN BY: ElectronNix



* (2) Intrarea U50/14 este folosita aici pentru "modificarea de 80K", primind o linie suplimentara de adresa video generata la pagina cu "Circuitul de configurare si selectie".

* (2) Input U50/14 is used here for the purpose of the "80K modification", receiving an extra video address line generated on the page with "Configurator and selector circuit".



* (2) Intrarea U39/6 este folosita aici pentru "modificarea de 80K", primind o linie suplimentara de adresa video generata la pagina cu "Modificari".

* (2) Input U39/6 is used here for the purpose of the "80K modification", receiving an extra video address line generated on the "Modifications" page.

* (1) U47-50 sint folosite aici pentru multiplexare liniilor de adresa catre memoria video SRAM. Multiplexarea este diferita de cea necesara pentru memoria video DRAM. Spre deosebire de cipurile DRAM, la SRAM nu mai e nevoie de multiplexare intre RAS si CAS, ci doar de multiplexare intre accesul controlerului video si cel al procesorului la memoria video.

Din diagrama din Fig.6 din manualul hardware se observa ca semnalul S0 poate fi folosit pentru a comanda multiplexarea intre adresele pentru RAS si adresele pentru CAS, iar semnalul STB poate fi folosit pentru a comanda multiplexarea intre adresele de la controlerul video si adresele de la procesor. Acest lucru este confirmat de schema originala a multiplexorului de adrese video, avind in vedere ca S0 este legat la bitul inferior de selectie a multiplexoarelor iar STB la cel superior si observind ca adresele de la controlerul video sint legate la intrarile 0 si 1 iar adresele de la procesor sint legate la intrarile 2 si 3.

Rezulta deci ca multiplexarea adreselor pentru SRAM (intre procesor si controler video) poate fi comandata de semnalul STB.

Aceste cipuri nu sint necesare daca nu se foloseste SRAM pentru memoria video.

* (1) U47-50 are used here for address multiplexing to the video SRAM memory.

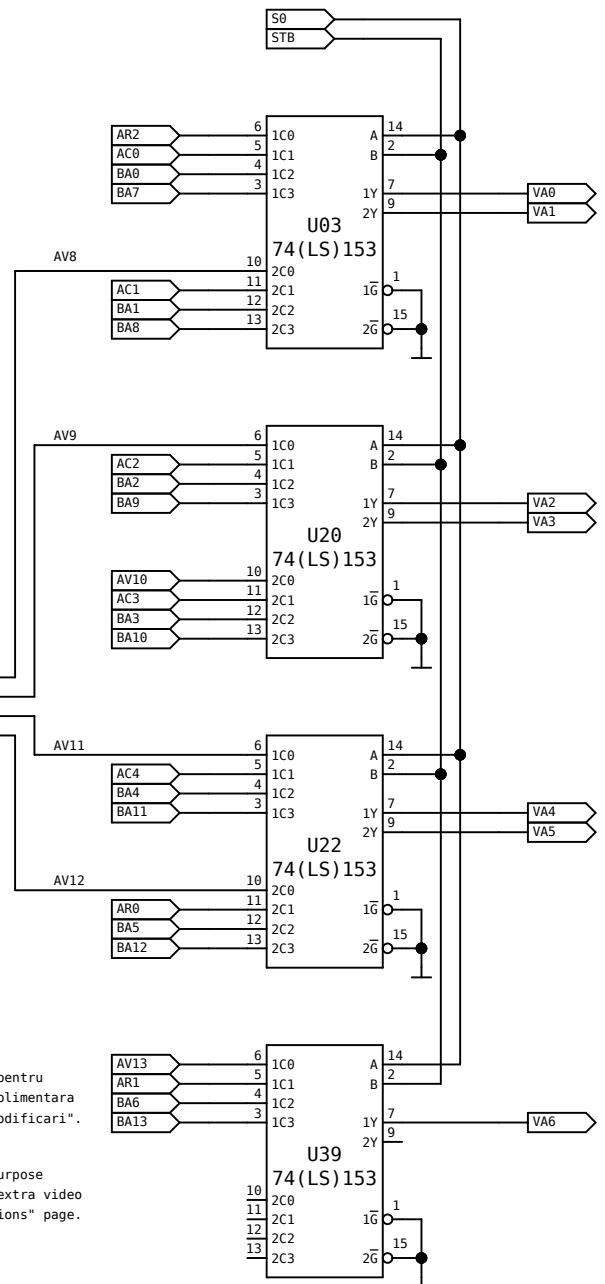
This multiplexing is different than the one required for the DRAM video memory.

Unlike the DRAM chips, SRAM does not require RAS / CAS multiplexing anymore, but only multiplexing between video controller and microprocessor accesses to video memory.

Examining Fig.6 in the hardware manual we can see that signal S0 can be used for driving the multiplexer between addresses for RAS and addresses for CAS, while signal STB can be used for driving the multiplexer between addresses from video controller and addresses from microprocessor. This is actually confirmed by examining the original schematic of the video address multiplexer, considering that S0 drives the lower selection bit of the the multiplexers and STB drives the higher one and noticing that the addresses from the video controller are connected to inputs 0 and 1 and the addresses from the microprocessor are connected to inputs 2 and 3.

In conclusion, address multiplexing for SRAM (between microprocessor and video controller) can be driven by signal STB.

These 4 IC's are not required if SRAM is not being used for the video memory.



TITLE μ C CoBra - Circuitul de multiplexare adrese video
CoBra μ C - Video address multiplexer circuit

FILE: CoBra

REVISION: 4.3 (80KB DRAM)

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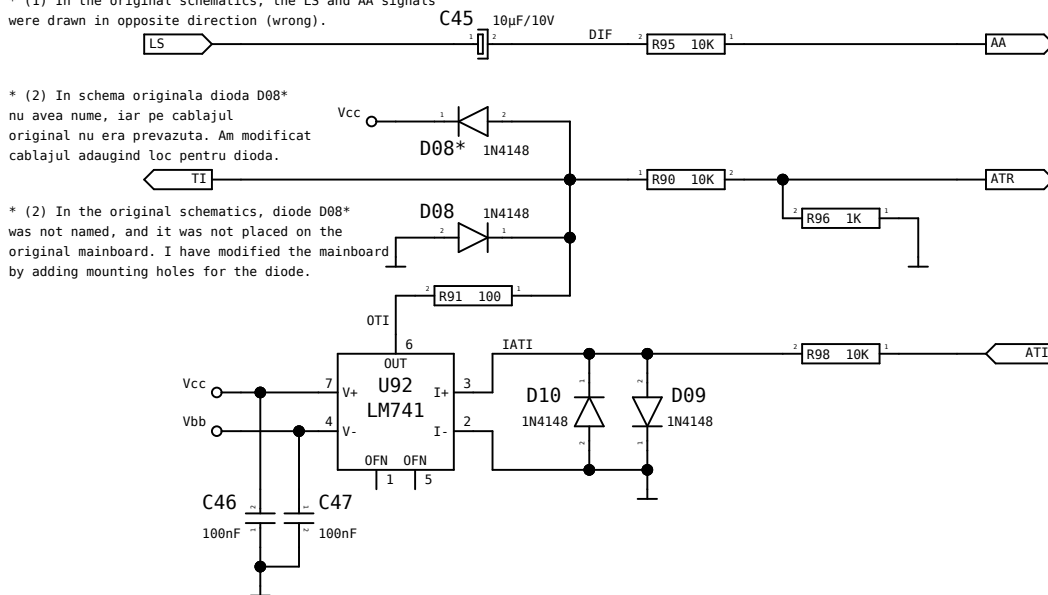
DRAWN BY: ElectroNnix

* (1) In schema originala semnalele LS si AA erau desenate in sens opus (gresit).

* (1) In the original schematics, the LS and AA signals were drawn in opposite direction (wrong).

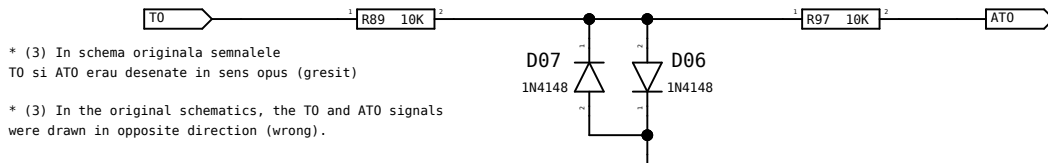
* (2) In schema originala dioda D08* nu avea nume, iar pe cablajul original nu era prevazuta. Am modificat cablajul adaugind loc pentru dioda.

* (2) In the original schematics, diode D08* was not named, and it was not placed on the original mainboard. I have modified the mainboard by adding mounting holes for the diode.



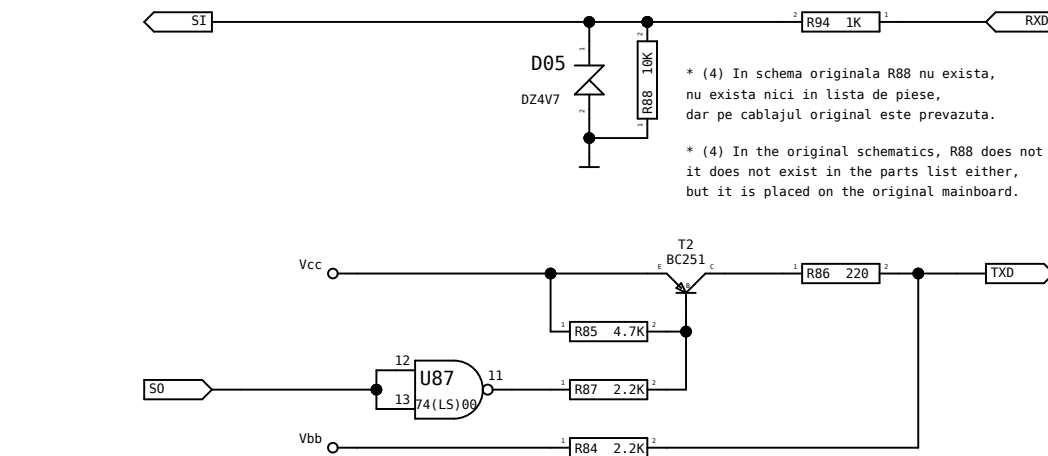
* (3) In schema originala semnalele T0 si ATO erau desenate in sens opus (gresit)

* (3) In the original schematics, the T0 and ATO signals were drawn in opposite direction (wrong).



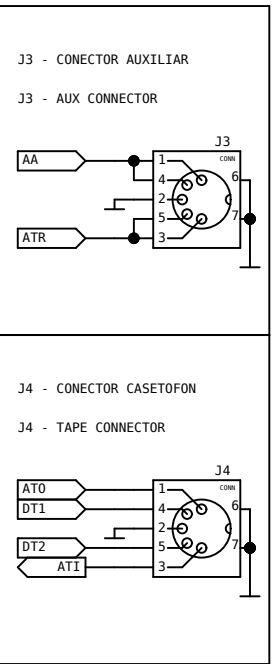
* (4) In schema originala R88 nu exista, nu exista nici in lista de piese, dar pe cablajul original este prevazuta.

* (4) In the original schematics, R88 does not exist, it does not exist in the parts list either, but it is placed on the original mainboard.



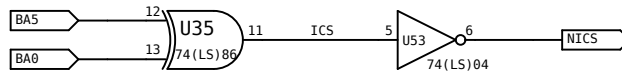
* (5) Pe cablajul original, poarta U87/13,12,11 era intercalata ca inversor intre U85/12 si U86/11, inversind semnalul I de la U85 la U86 (gresit). Am modificat deci cablajul conform acestei scheme (originale, corecte). (Vezi taieturile #1 si #2 de pe fata 1, #20 si #24 de pe fata 2, si legaturile #18, #20 si #21 de pe fata 2)

* (5) On the original PCB, gate U87/13,12,11 was placed as inverter between U85/12 and U86/11, inverting the signal I from U85 to U86 (wrong). I have therefore changed the mainboard layout according to the original (correct) schematic (shown here). (See cuts #1 & #2 on side 1, #20 & #24 on side 2, and rewirings #18, #20 & #21 on side 2)



TITLE		µC CoBra - Circuite de adaptare nivel CoBra µC - Voltage-level adapter circuits	
FILE:	CoBra	REVISION:	4.21 (ROM upgrade, 64KB DRAM)
PAGE	16 OF 19	DRAWN BY:	ElectroNNix

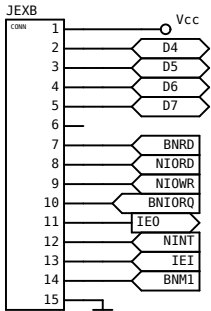
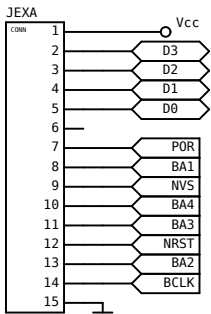
* (1) Pe cablajul original JEXA/8 este legat in mod gresit la BA7.
De asemenea, manualul original avea JEXA/8 listat ca fiind legat la BA7. Am modificat deci cablajul si schema de fata legind JEXA/8 la BA1 (corect).
(Vezi taietura #11 fata 1, legatura #22 fata 2)



* (1) On the original mainboard, JEXA/8 was connected (the wrong way) to BA7. Also the original hardware manual had JEXA/8 listed as being connected to BA7. I have therefore changed the mainboard layout and this schematic by connecting JEXA/8 to BA1 (correctly).
(See cut #11 side 1, rewiring #22 side 2)

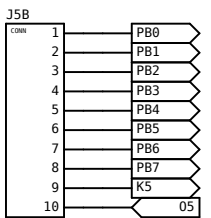
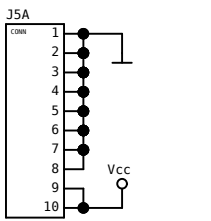
JEXA+B - CONECTOR INTERFATA FLOPPY DISK

JEXA+B - FLOPPY DISK INTERFACE CONNECTOR



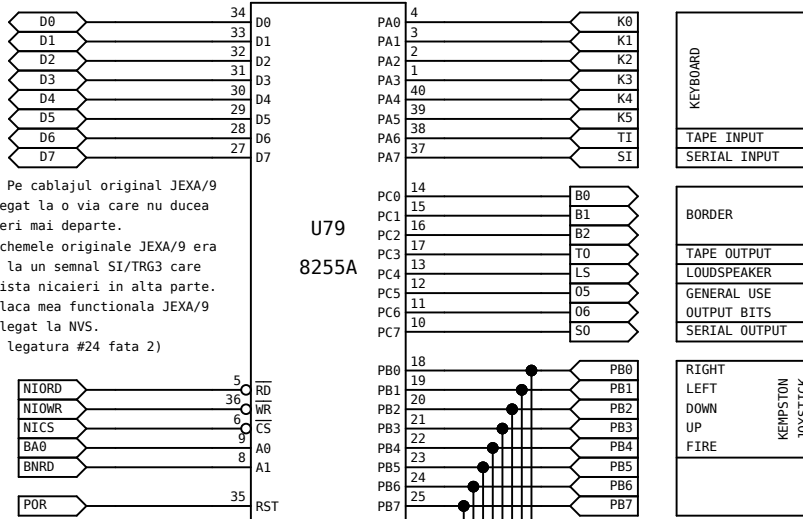
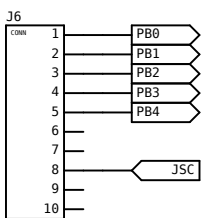
J5A+B - CONECTOR PORT INTRARE PE 8 BITI ADRESA 0DFH

J5A+B - 8-BIT INPUT PORT 0DFH CONNECTOR



J6 - CONECTOR JOYSTICK KEMPSTON

J6 - KEMPSTON JOYSTICK CONNECTOR

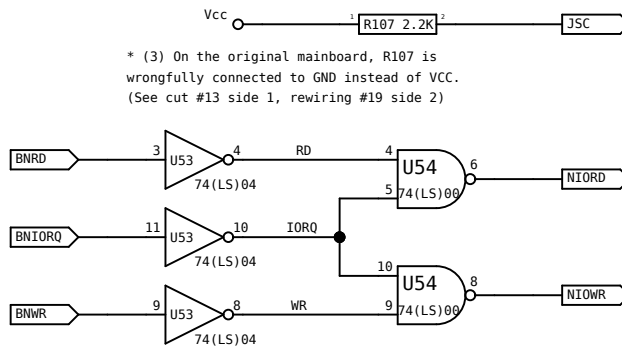


* (2) Pe cablajul original JEXA/9 era legat la o via care nu ducea nicaieri mai departe. In schemele originale JEXA/9 era legat la un semnal SI/TRG3 care nu exista nicaieri in alta parte. Pe placa mea functionala JEXA/9 este legat la NVS.
(Vezi legatura #24 fata 2)

* (2) On the original mainboard, JEXA/9 was connected to a via which was not further leading anywhere. In the original schematics, JEXA/9 was connected to a signal "SI/TRG3" which did not exist anywhere else. On my working mainboard, JEXA/9 is connected to NVS.
(See rewiring #24 side 2)

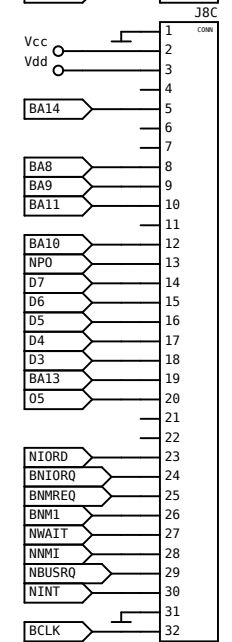
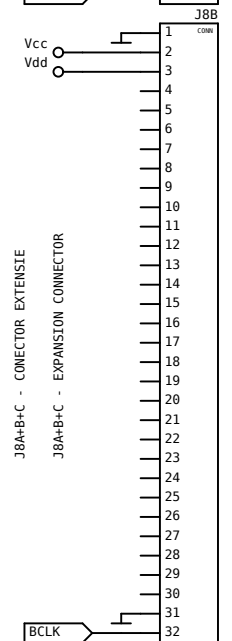
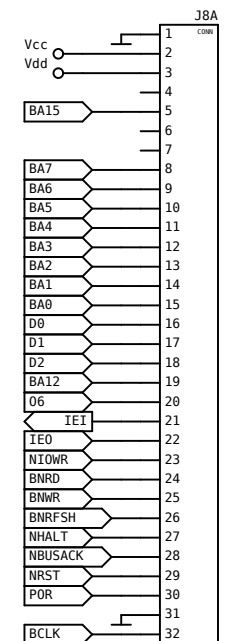
* (3) Pe cablajul original, R107 este legata in mod gresit la GND in loc de VCC.
(Vezi taietura #13 fata 1, legatura #19 fata 2)

* (3) On the original mainboard, R107 is wrongfully connected to GND instead of VCC.
(See cut #13 side 1, rewiring #19 side 2)



* (4) Cablajul original avea JSC conectat la J6/pin10 dar manualul original avea JSC listat la J6/pin8. Am schimbat cablajul placii de baza pentru a corespunde manualului.
(Vezi taietura #5 fata 1, legatura #1 fata 1)

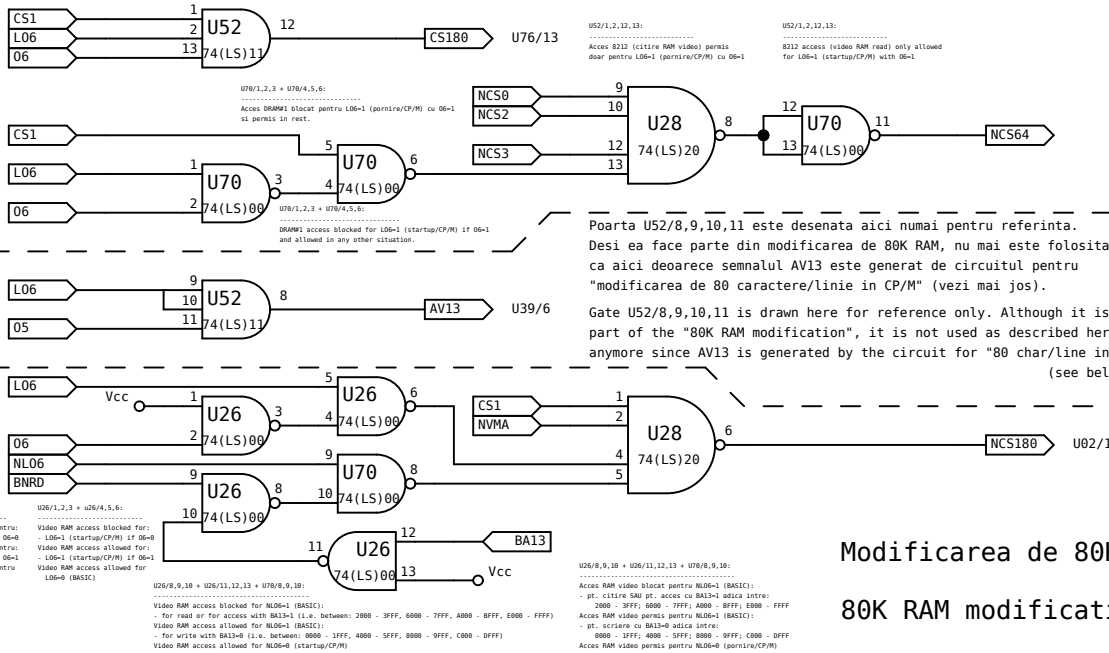
* (4) The original mainboard had JSC connected to J6/pin10 but the original manual had JSC listed at J6/pin8. I changed the mainboard layout to match the original manual.
(See cut #5 side 1, rewiring #1 side 1)



TITLE μ C CoBra - Interfete
CoBra μ C - Interfaces

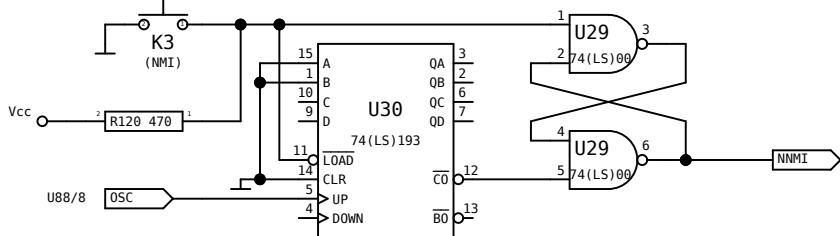
FILE: CoBra
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REVISION: 4.21 (ROM upgrade, 64KB DRAM)
DRAWN BY: ElectronNix



Poarta U52/8,9,10,11 este desenata aici numai pentru referinta. Desi ea face parte din modificarea de 80K RAM, nu mai este folosita ca aici deoarece semnalul AV13 este generat de circuitul pentru "modificarea de 80 caractere/linie in CP/M" (vezi mai jos). Gate U52/8,9,10,11 is drawn here for reference only. Although it is part of the "80K RAM modification", it is not used as described here anymore since AV13 is generated by the circuit for "80 char/line in CP/M". (see below)

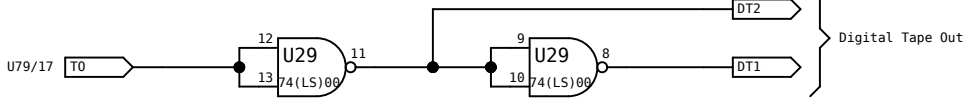
Modificarea de 80K RAM 80K RAM modification



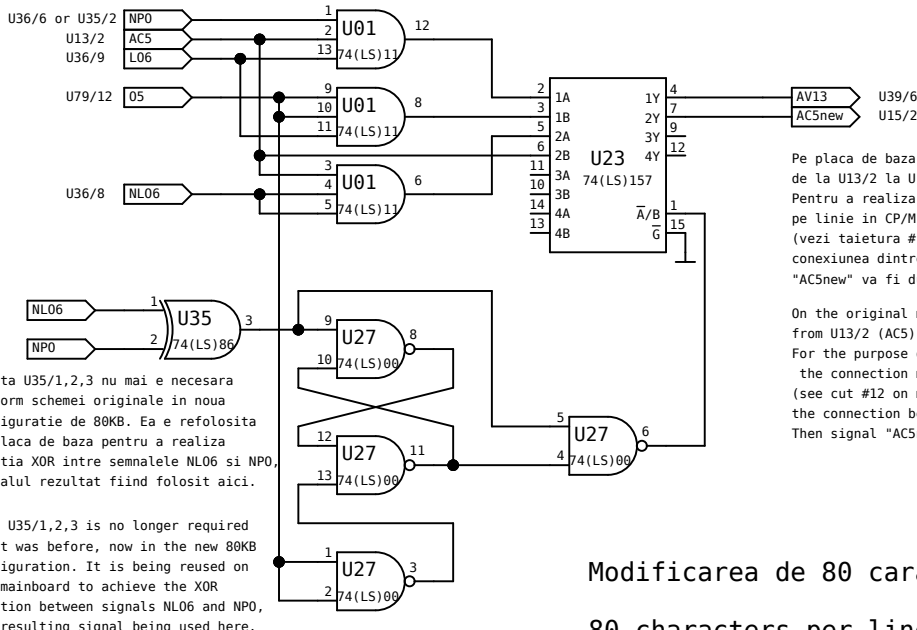
NMI Button Circuit Circuit pentru buton NMI

Intrarea \overline{NMI} a procesorului fiind activa pe frontul negativ al semnalului, acest circuit asigura aplicarea unui singur front negativ, evitand inputuri parazite datorate unui eventual switch imperfect. The \overline{NMI} input to the 286 CPU being active on the negative edge of the signal, this circuit makes sure only one negative edge is applied, avoiding unwanted multiple transitions due to a possibly imperfect switch.

Semnal digital de iesire pt. caseta (simetric, mai puternic)



"Digital" Tape Out signal (symmetrical, stronger)



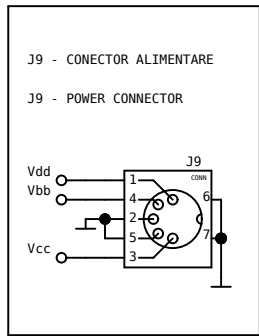
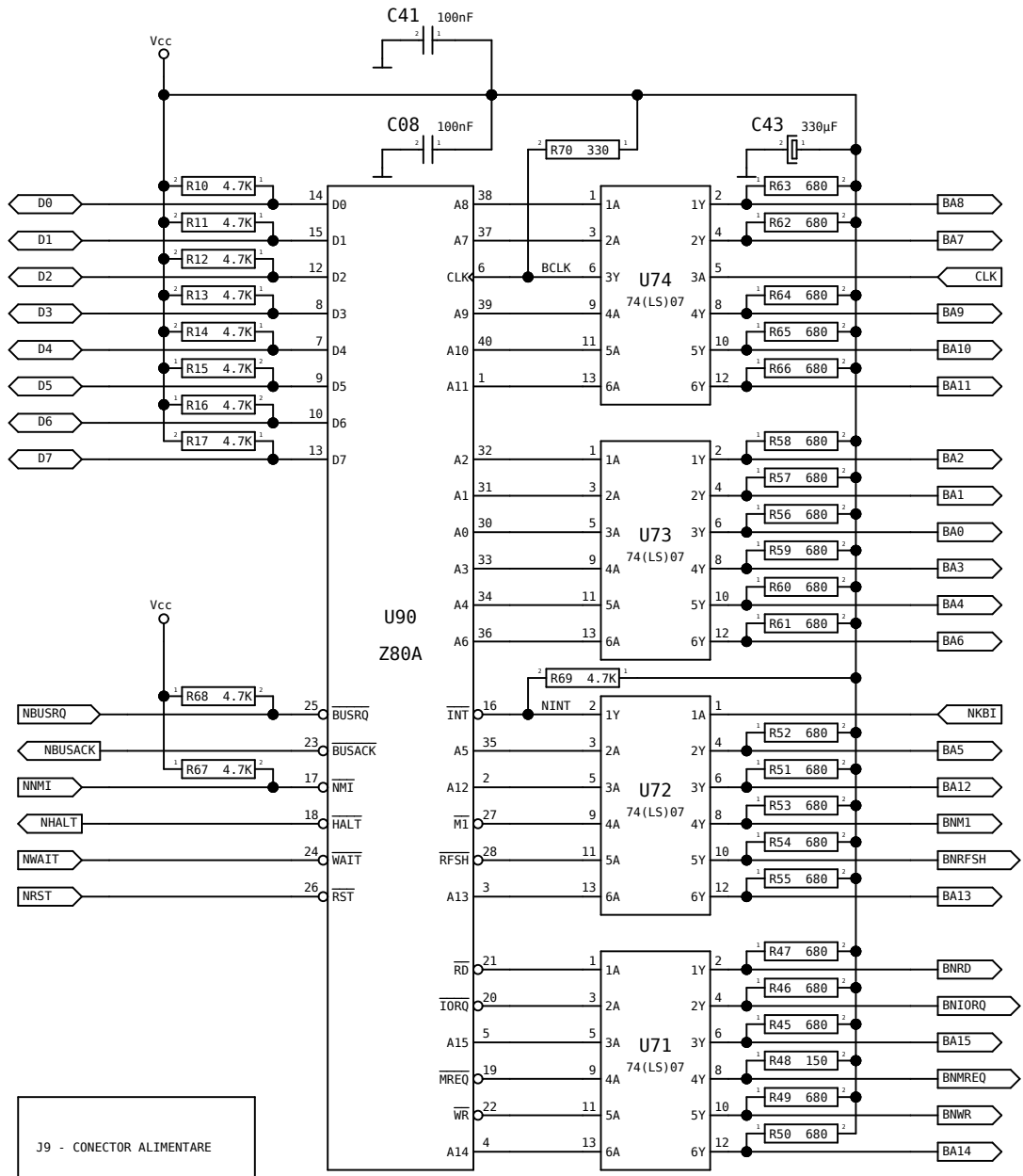
Pe placa de baza originala fata 1, exista un traseu de la U13/2 la U14/2,9 si apoi la U15/2. Pentru a realiza "modificarea de 80 caractere pe linie in CP/M" traseul trebuie taiat imediat linga U15/2, (vezi taietura #12 pe fata 1 a placii de baza), pastrand conexiunea dintre U13/2 si U14/2,9. Apoi semnalul "AC5new" va fi dus la U15/2, On the original mainboard side 1, there is a connection from U13/2 (AC5) to U14/2,9 and further to U15/2. For the purpose of the "80 char/line in CP/M modification" the connection must be cut right next to U15/2 (see cut #12 on mainboard side 1), preserving the connection between U13/2 and U14/2,9. Then signal "AC5new" will be routed to U15/2.

Modificarea de 80 caractere pe linie in CP/M 80 characters per line in CP/M modification

TITLE		µC CoBra - Modificari CoBra µC - Modifications	
FILE:	CoBra	REVISION:	4.3 (80KB DRAM)
PAGE	18 OF 19	DRAWN BY:	ElectroNnix

* (1) In schema originala, U74/6 era legat (gresit) la U90/24, dar corect este ca U90/24 sa fie legat la NWAIT, U74/6 (BCLK) sa fie legat la U90/6 (CLK procesor) si U74/5 sa fie legat la CLK

* (1) In the original schematics, U74/6 was connected (wrong) to U90/24, but correct is for U90/24 to be connected to NWAIT, for U74/6 (BCLK) to be connected to U90/6 (CPU clock) and for U74/5 to be connected to CLK



* (2) In schema originala, R48 era plasata pe pagina cu circuitul memoriei dinamice.

* (2) In the original schematics, R48 was drawn on the page with the dynamic memory circuit.

TITLE		µC CoBra - Unitatea centrala CoBra µC - Central Processing Unit	
FILE:	CoBra	REVISION:	3 (original design, 64KB DRAM)
PAGE	19 OF 19	DRAWN BY:	ElectroNNix