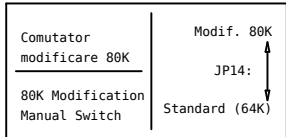


\* (4) In practice CVR and CCS were not required, but only CCC which for 120 ns access time DRAM had a value of 560 pF.



\* (1) Functional vorbind, poarta U19/1,2,3 este inutila.  
 \* (1) Functionally speaking, gate U19/1,2,3 is useless.

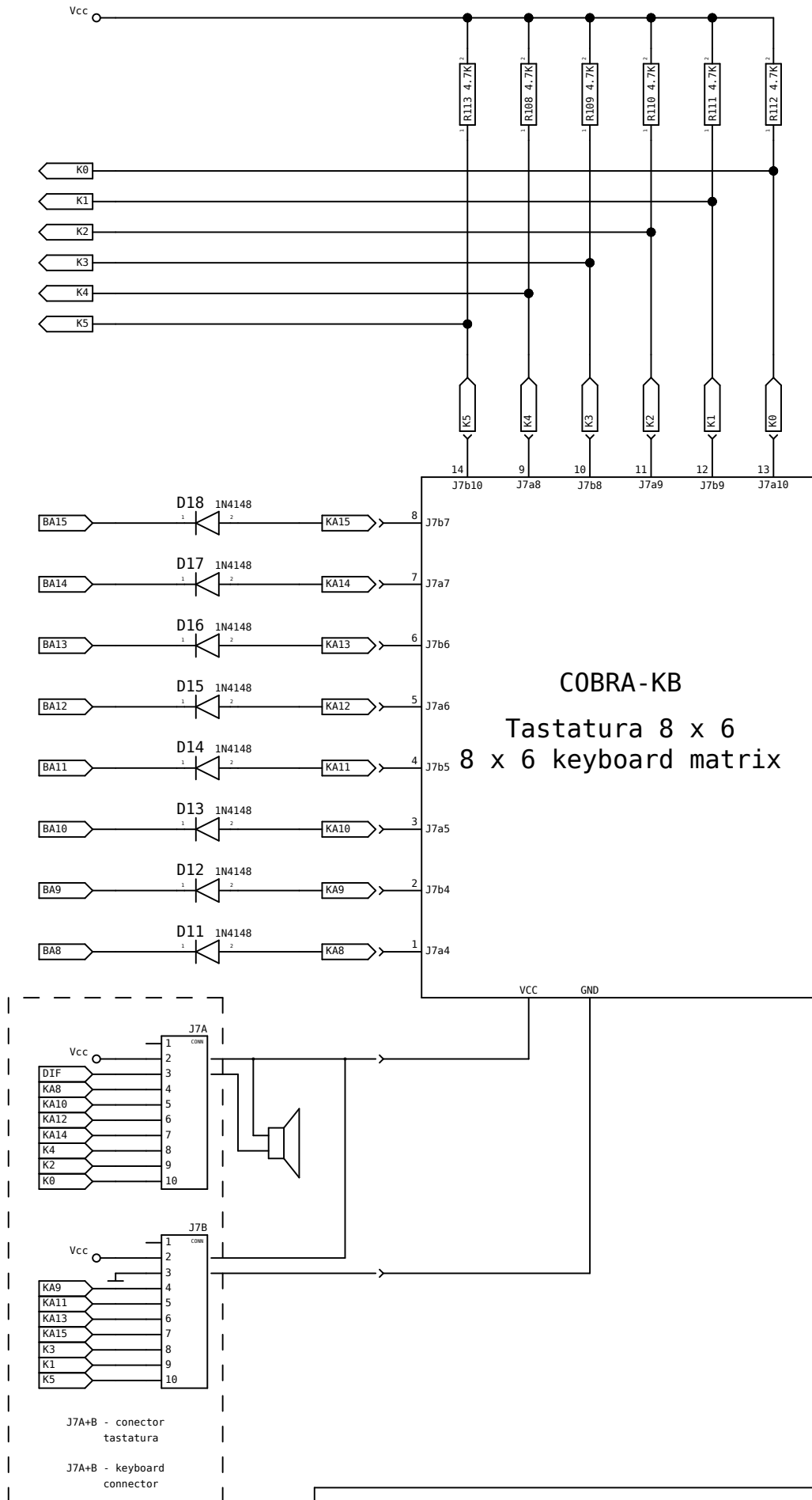
\* (2) CCS apare in schema originala, dar pe cablajul original nu este prevazut.

\* (2) CCS exists in the original schematics, but does not exist on the original mainboard.

\* (3) In schema originala, U02/3 este legat (gresit) la QD (U60/10) dar pe cablajul original este legat (corect) la QC (U60/11).

\* (3) In the original schematics, U02/3 is connected (wrong) to QD (U60/10), but on the original mainboard it is connected (correctly) to QC (U60/11).

TITLE		μC CoBra - Arbitrul de memorie si logica de comanda	
		CoBra μC - Memory access prioritizer and command logic	
FILE:	CoBra	REVISION:	3.16a (test, 64/80KB DRAM)
PAGE	1 OF 16	DRAWN BY:	ElectroNNix



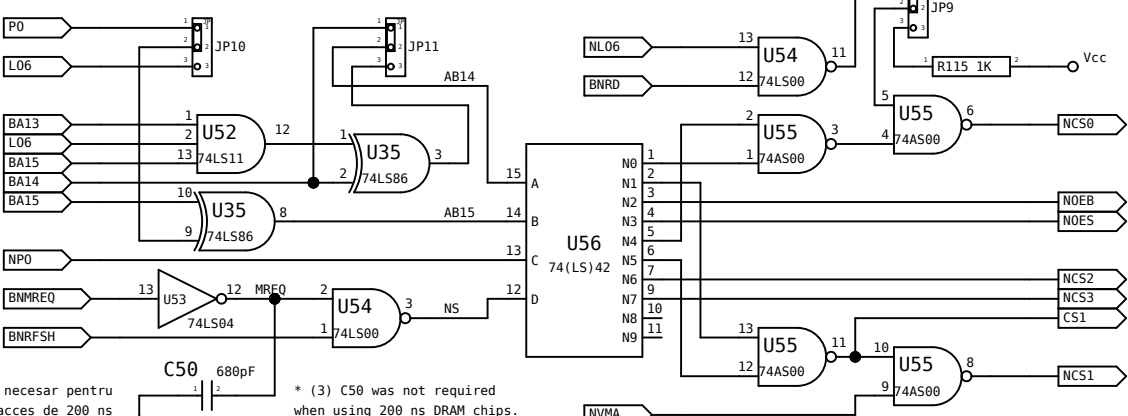
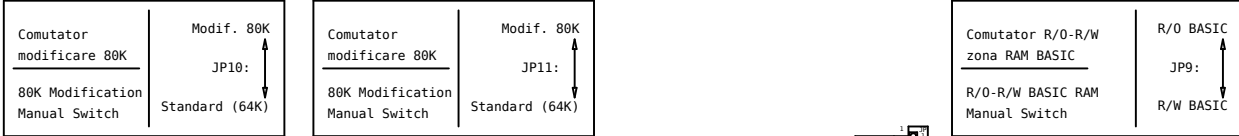
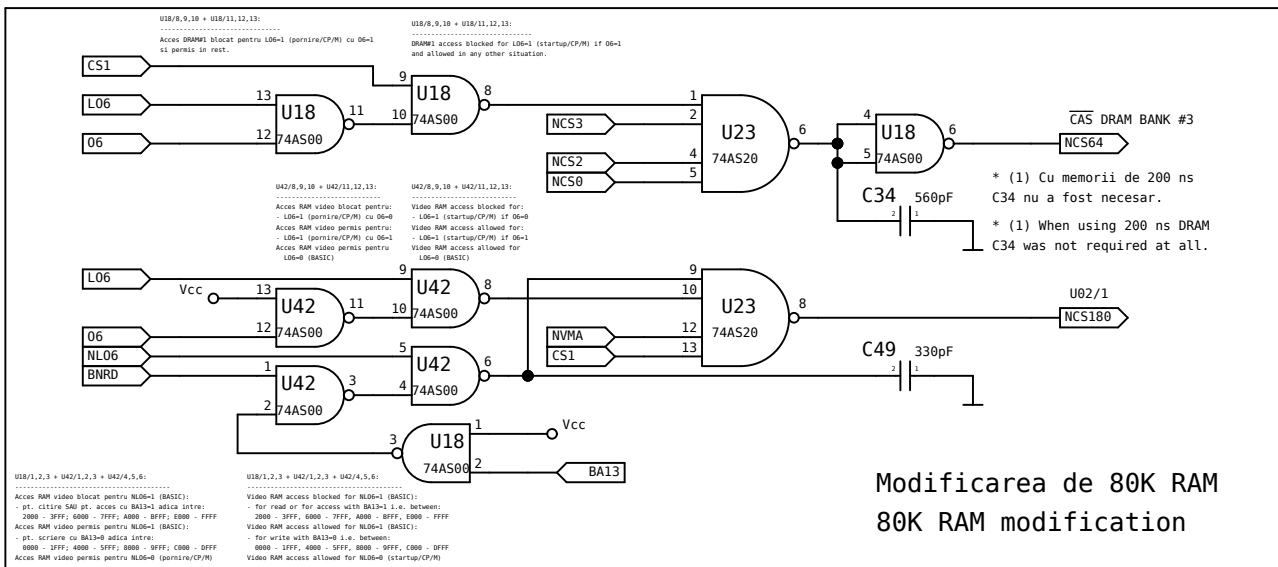
TITLE  $\mu$ C CoBra - Circuitul de conectare tastatura  
CoBra  $\mu$ C - Keyboard interfacing circuit

FILE: CoBra

REVISION: 3 (original design, 64KB DRAM)

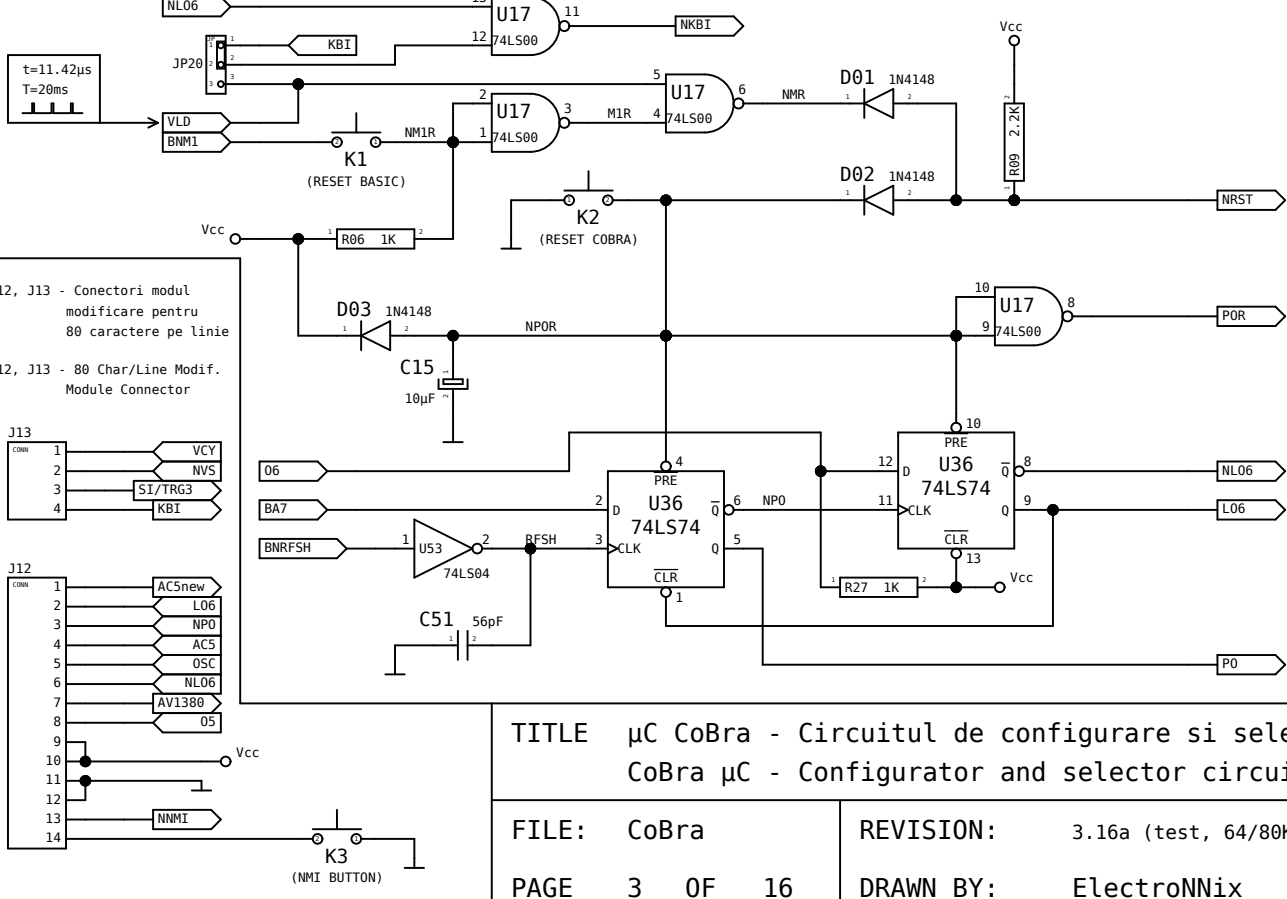
PAGE 2 OF 16

DRAWN BY: ElectronNix



\* (2) In the original schematics, input U17/12 was connected to VCY inverted through U52/6, (U52 being a 74(LS)10 (3 NOR 3-input gates)) but on the original mainboard (correctly) it is connected to U17/5 (which is connected to VLD).

\* (2) In schema originala, intrarea U17/12 era legata la VCY inversat prin U52/6, (U52 fiind un 74(LS)10 (3 porti NOR cu 3 intrari)) dar pe cablaj (corect) este legata la U17/5 (care este legat la VLD).



**\* (3) IMPORTANT!**

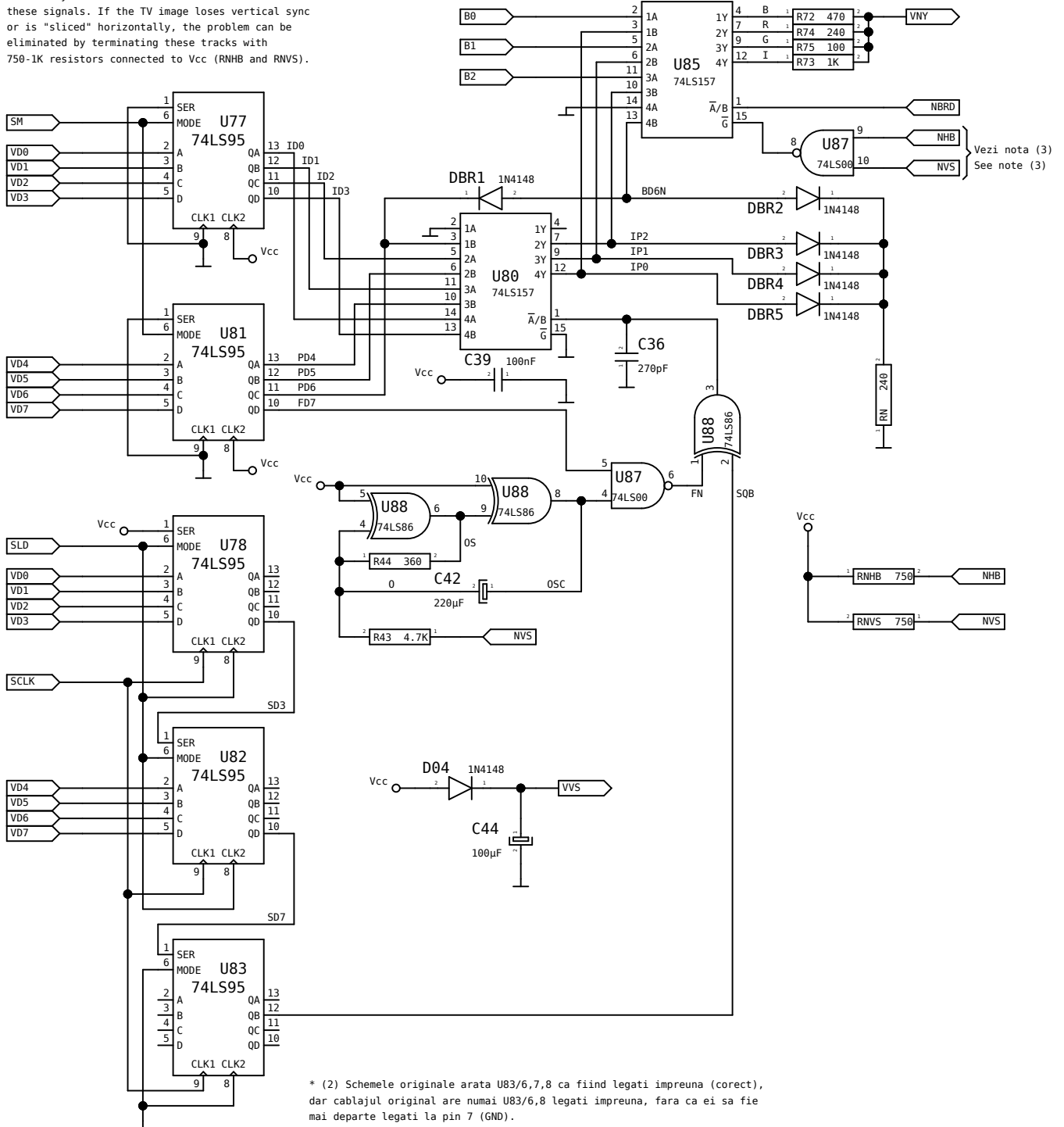
Semnalele NHB si NVS vin la acest circuit video prin trasee destul de lungi, care trec prin mijlocul blocului de memorii. De aceea e posibil sa apara perturbatii. In caz ca imaginea se desincronizeaza pe verticala sau se feliaza pe orizontala, situatia se remediaza prin terminarea acestor trasee cu rezistori de 750-1K legati la Vcc (RNHB si RNVS).

**\* (3) IMPORTANT!**

Signals NHB and NVS get to this video circuit through some pretty long tracks, which cross the memory block. Therefore noise can distort these signals. If the TV image loses vertical sync or is "sliced" horizontally, the problem can be eliminated by terminating these tracks with 750-1K resistors connected to Vcc (RNHB and RNVS).

\* (1) In schema originala, diodele DBR1-5 si rezistenta RN sint desenate (cu toate ca diodele nu sint denumite) dar pe cablajul original nu sint prevazute, iar U85/13 este legat direct la U80/3. Ca urmare, cablajul original nu permitea functia de BRIGHT. Am modificat cablajul adaugind gauri pentru DBR1-5 si RN si intrerupind deci legatura directa dintre U85/13 si U80/3.

\* (1) In the original schematics, diodes DBR1-5 and resistor RN are drawn (although the diodes don't have names) but on the original mainboard they are not placed, and U85/13 is directly connected to U80/3. Therefore, the original mainboard would not allow the BRIGHT function. I have modified the mainboard layout by adding mounting holes for DBR1-5 and RN and therefore interrupting the direct connection between U85/13 and U80/3.



\* (2) Schemele originale arata U83/6,7,8 ca fiind legati impreuna (corect), dar cablajul original are numai U83/6,8 legati impreuna, fara ca ei sa fie mai departe legati la pin 7 (GND). Am modificat cablajul placii de baza pentru a corespunde schemei originale. (Vezi legatura #25 fata 2).

\* (2) The original schematics show U83/6,7,8 connected together (correctly), but the original mainboard layout only has U83/6,8 connected together without them being further connected to pin 7 (GND). I have modified the mainboard layout to match the original schematics. (See rewiring #25 side 2).

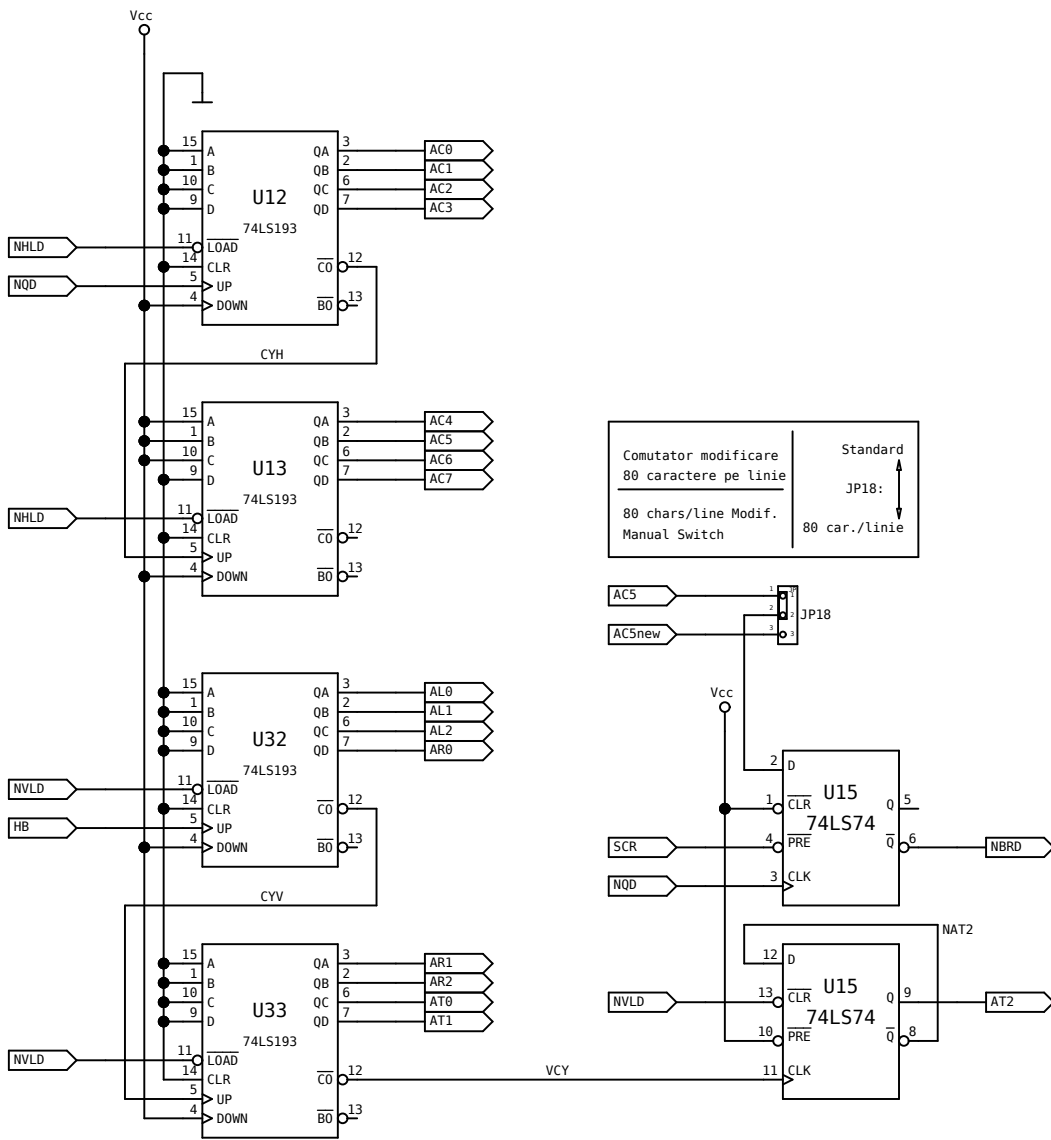
TITLE  $\mu$ C CoBra - Circuitul formator semnal video  
CoBra  $\mu$ C - Video signal generator circuit

FILE: CoBra

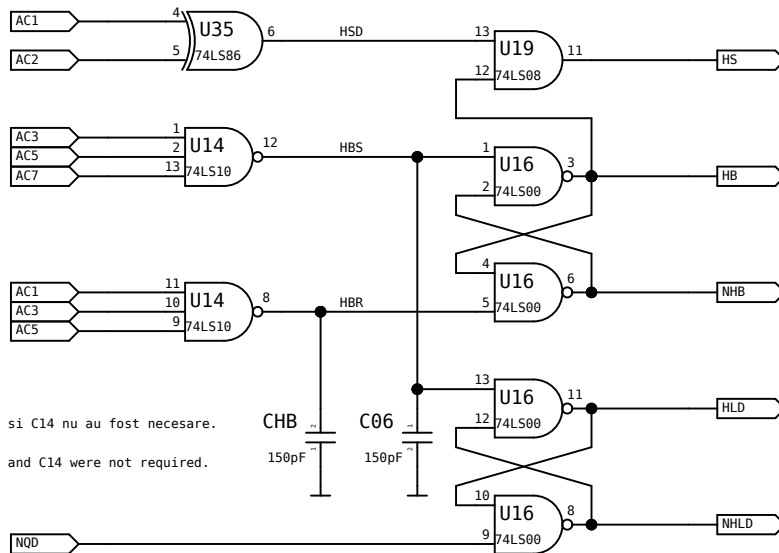
REVISION: 3.16a (test, 64/80KB DRAM)

PAGE 4 OF 16

DRAWN BY: ElectroNnix

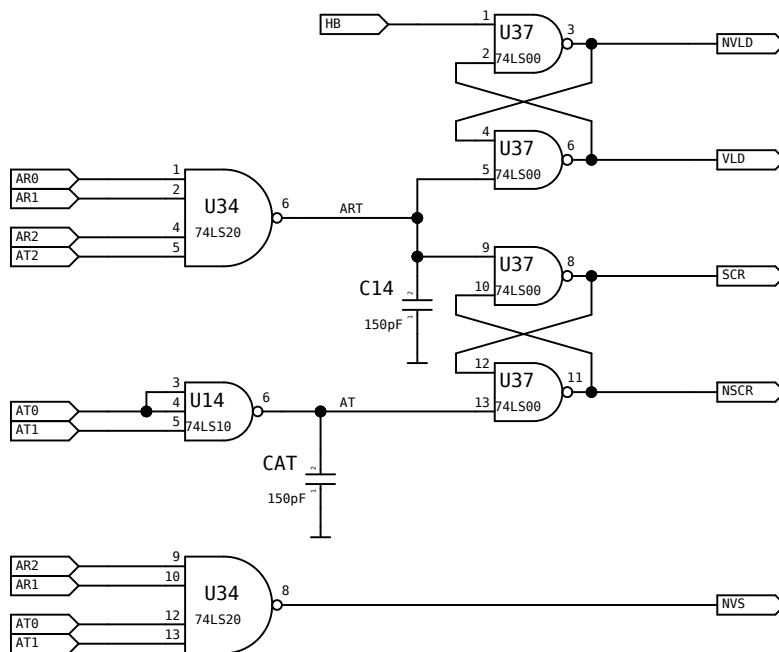


TITLE		μC CoBra - Circuitul de generare adrese video CoBra μC - Video address generator circuit	
FILE:	CoBra	REVISION:	3.16a (test, 64/80KB DRAM)
PAGE	5 OF 16	DRAWN BY:	ElectroNnix

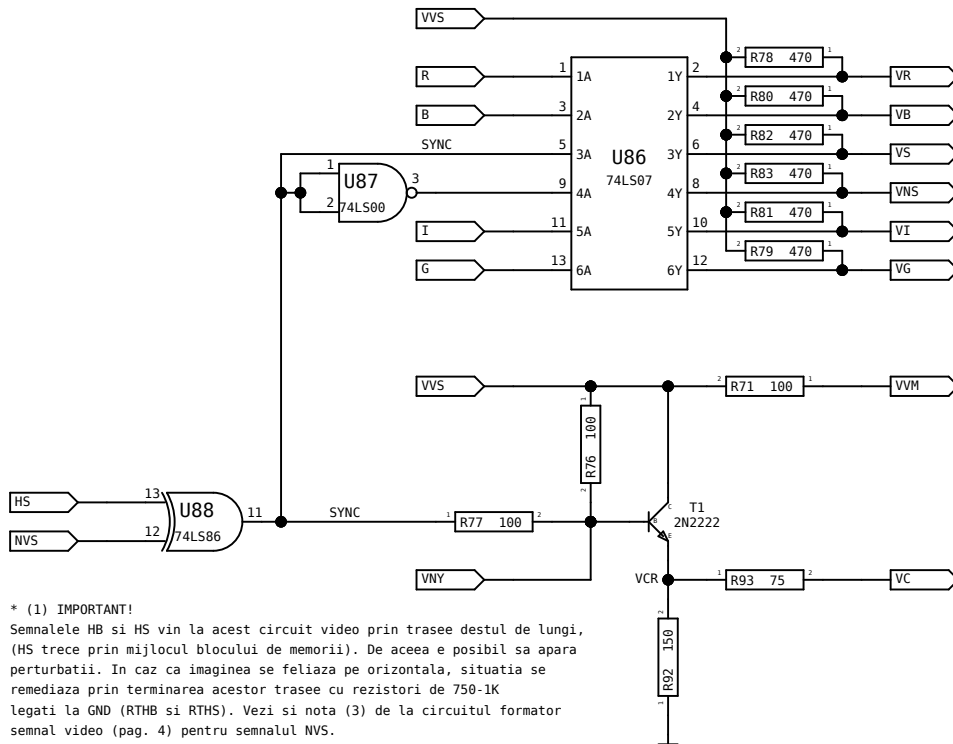


\* (1) In practica CHB, CAT, C06 si C14 nu au fost necesare.

\* (1) In practice CHB, CAT, C06 and C14 were not required.

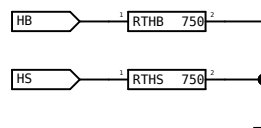


TITLE		μC CoBra - Circuitul generator de sincroimpulsuri CoBra μC - Video sync pulses generator circuit	
FILE:	CoBra	REVISION:	3 (original design, 64KB DRAM)
PAGE	6 OF 16	DRAWN BY:	ElectroNNix

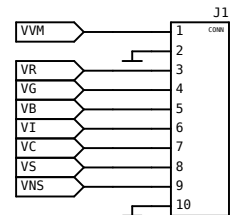


\* (1) IMPORTANT!  
 Semnalele HB si HS vin la acest circuit video prin trasee destul de lungi, (HS trece prin mijlocul blocului de memorii). De aceea e posibil sa apara perturbatii. In caz ca imaginea se feliaza pe orizontala, situatia se remediaza prin terminarea acestor trasee cu rezistori de 750-1K legati la GND (RTHB si RTHS). Vezi si nota (3) de la circuitul formator semnal video (pag. 4) pentru semnalul NVS.

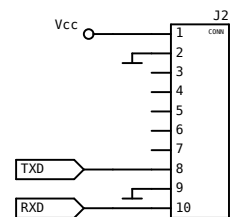
\* (3) IMPORTANT!  
 Signals HB and HS arrive to this video circuit through pretty long tracks, (HS crosses the memory block). Therefore noise can distort this signal. If the TV image is "sliced" horizontally, the problem can be eliminated by terminating these track with 750-1K resistors connected to GND (RTHB and RTHS). See also note (3) at page 4, (the Video Signal Generator Circuit), regarding signal NVS.



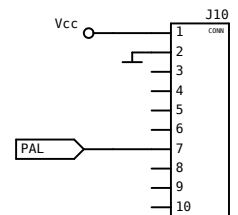
J1 - CONECTOR VIDEO  
 J1 - VIDEO CONNECTOR



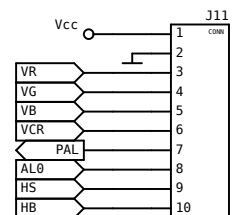
J2 - CONECTOR RS232  
 J2 - RS232 CONNECTOR



J10 - CONECTOR PAL VIDEO  
 J10 - PAL VIDEO CONNECTOR



J11 - CONECTOR CODOR PAL  
 J11 - PAL CODER CONNECTOR



TITLE  $\mu$ C CoBra - Circuitul de interfata cu monitorul TV  
 CoBra  $\mu$ C - TV monitor interfacing circuit

FILE: CoBra

REVISION: 3.16a (test, 64/80KB DRAM)

PAGE 7 OF 16

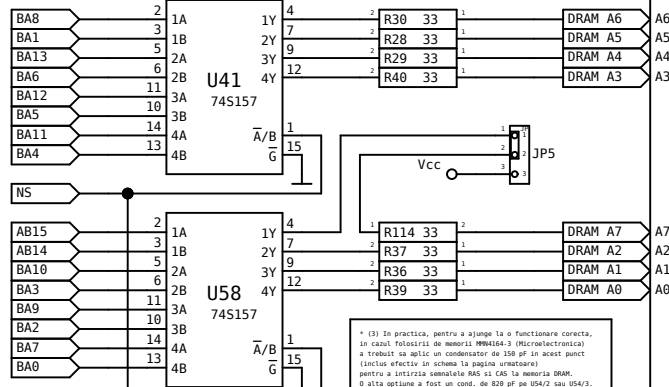
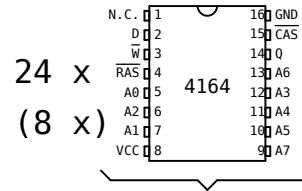
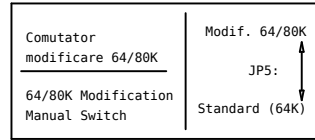
DRAWN BY: ElectroNnix

\* (2) In practica am facut teste cu doua tipuri de memorii: cu timp de acces de 120 ns si de 200 ns. Experimental am constatat ca pentru timpi de acces mari (200 ns) U41 si U58 trebuie sa fie 74LS157 (timp de propagare mic), iar pentru timpi de acces mici (120 ns) trebuie sa fie 74LS157 (timp de propagare mare). Totusi memoriile de 120 ns n-au functionat corect in nici un caz in cadrul acestui circuit de memorie sistem. Concluzia: acest circuit necesita memorii DRAM cu timp de acces mare (150-200 ns, 200 ns e valoarea optima).

\* (2) In practice I did tests with 2 types of memories: 120 ns and 200 ns access time. Experimentally I found that for high access times (200 ns) U41 and U58 must be 74LS157 (low propagation time), and for low access times (120 ns) they must be 74LS157 (high propagation time). Yet the 120 ns memories never worked properly. Conclusion: this circuit requires DRAM memories with high access time (150-200 ns, 200 ns would be the optimal value).

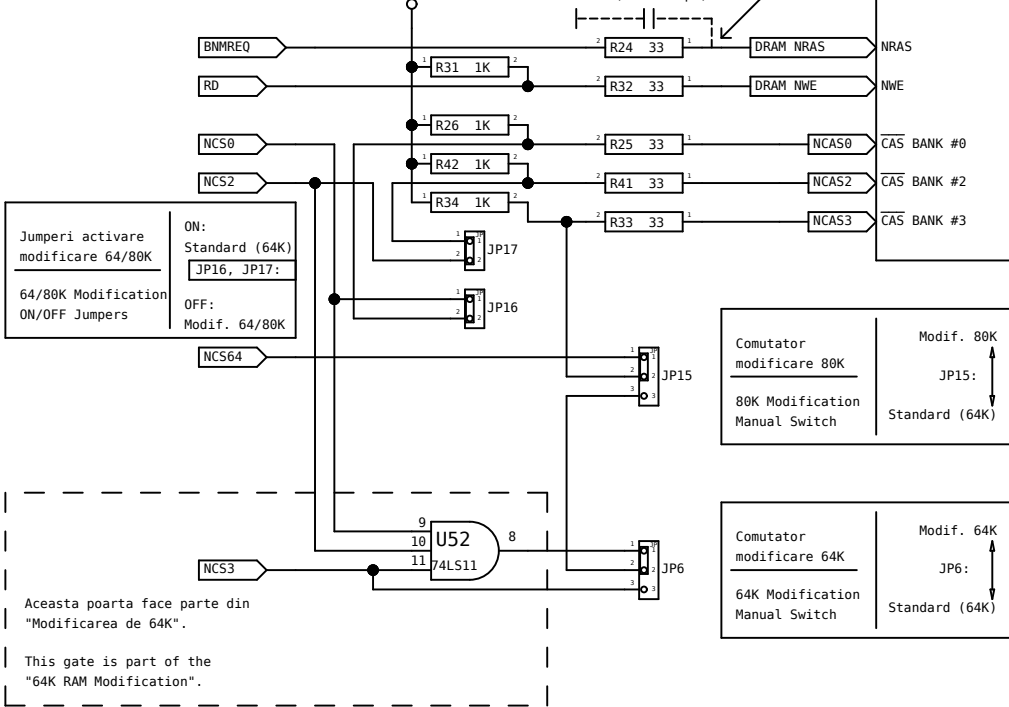
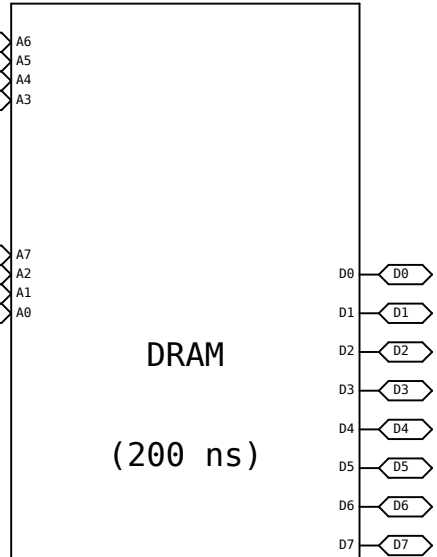
\* (1) Memorii de 64K x 1 bit. In configuratia standard sint folosite ca memorii de 16K x 1 bit (A7 legat la VCC) si toate bancurile (0, 2, 3) sint ocupate (24 cipuri folosite). In configuratia modificarii de 64K sau 80K, linia de adresa A7 este folosita si numai bancul 3 este ocupat (8 cipuri folosite).

\* (1) 64K x 1 bit memories. In standard configuration they are used as 16K x 1 bit memories (A7 kept at "1") and all memory banks (0, 2, 3) are used (24 chips used). In the "64K / 80K Modification" configuration, DRAM address line A7 is used and only memory bank 3 is used (8 memory chips used).

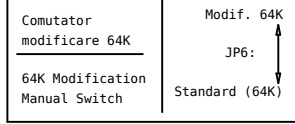
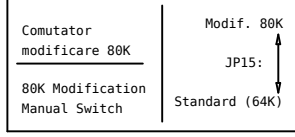


U58/2,3,4+R114 fac parte din "Modificarea de 64K" si de asemenea din "Modificarea de 80KB RAM" (adresabili integral).  
U58/2,3,4+R114 are part of the "64K Modification" and also of the "80K RAM Modification" (fully addressable).

\* (3) In practica, pentru a ajunge la o functionare corecta, in cazul folosirii de memorii MM5164-3 (Microelectroonica) a trebuit sa aplic un condensator de 150 pF in acest punct (inclus efectiv in schema la pagina urmatoare) pentru a intarzia semnalul RAS si CAS la memoria DRAM. O alta optiune a fost un cond. de 820 pF pe U54/2 sau U54/3. In cazul folosirii de memorii TMS4164-20 (200 ns) nu a mai fost nevoie de nici un condensator de intarziere pe RAS sau CAS.  
\* (3) In practice, in order to get to a correct operation, when using MM5164-3 memories (Microelectronics) I had to apply a 150 pF capacitor to this point (actually included in the schematic on the next page) to delay the RAS and CAS signals to the DRAM memory. Another option was an 820 pF capacitor applied on U54/2 or U54/3. When using TMS4164-20 (200 ns) memories, no delay capacitors were required anymore for RAS or CAS.

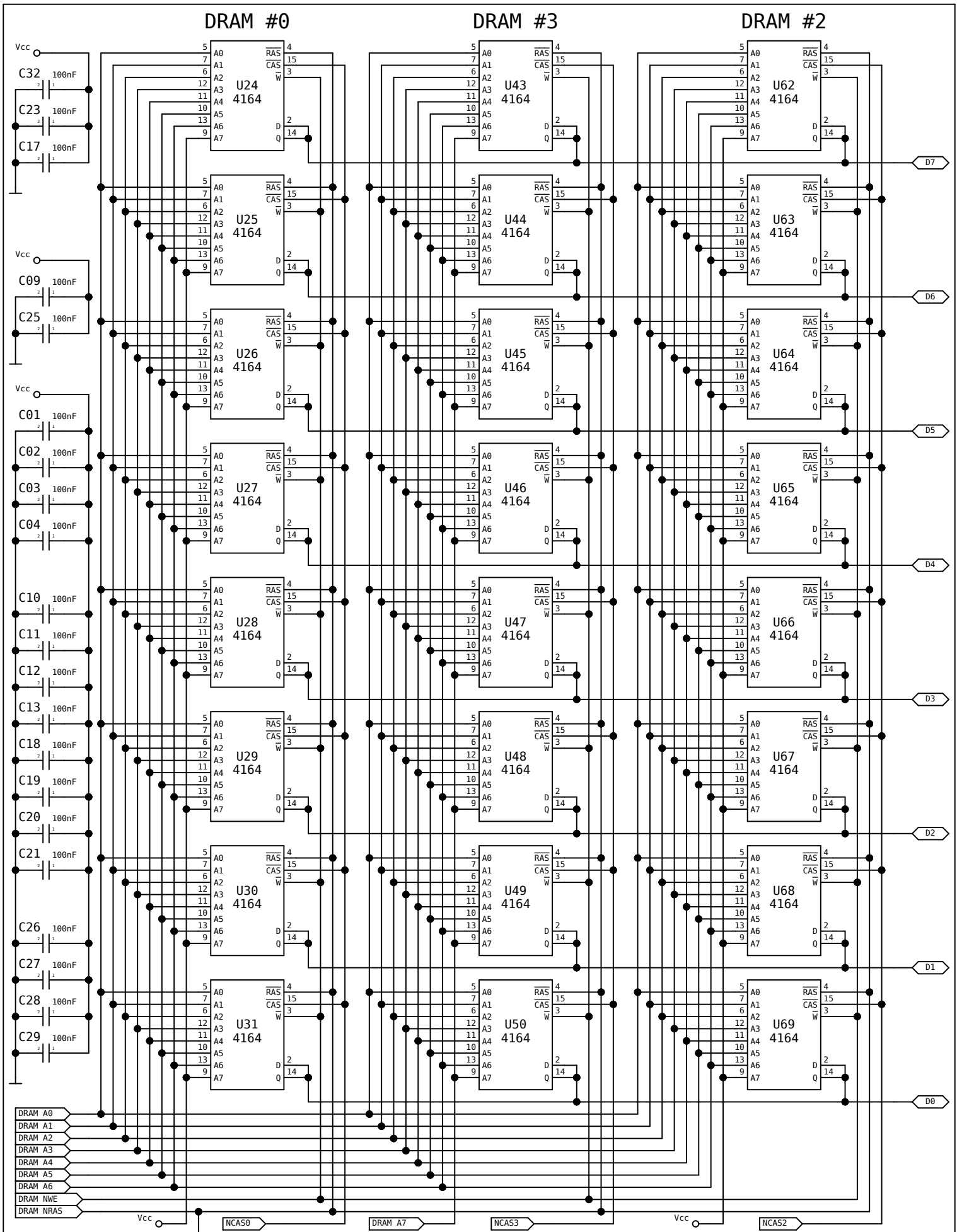


Aceasta poarta face parte din "Modificarea de 64K".  
This gate is part of the "64K RAM Modification".



TITLE		µC CoBra - Circuitul memoriei dinamice - pag.1/2	
		CoBra µC - Dynamic memory circuit - pag.1/2	
FILE:	CoBra	REVISION:	3.16a (test, 64/80KB DRAM)
PAGE	8 OF 16	DRAWN BY:	ElectroNNix





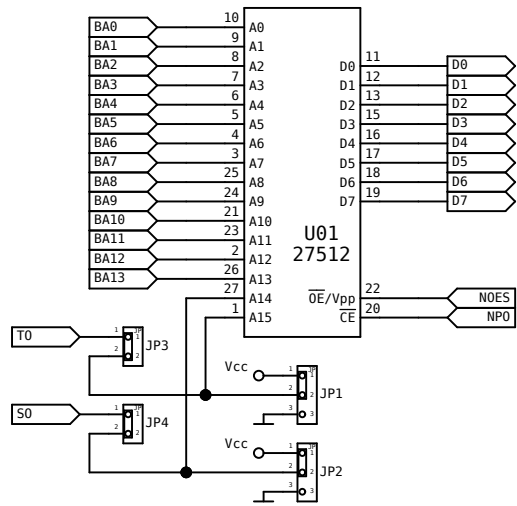
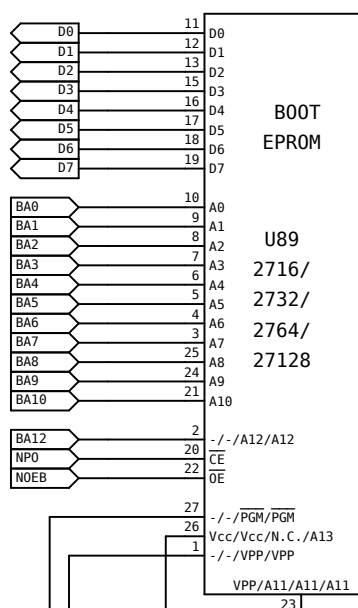
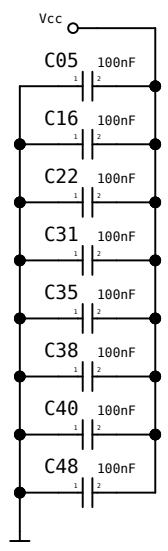
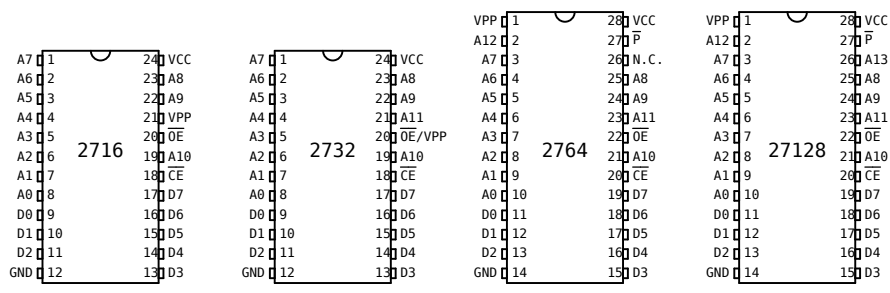
Vbb

C33 100nF

C52 150pF

\* (1) Cu memorii de 200 ns, C52 nu a fost necesar.

\* (1) For 200 ns DRAM, C52 was not required at all.

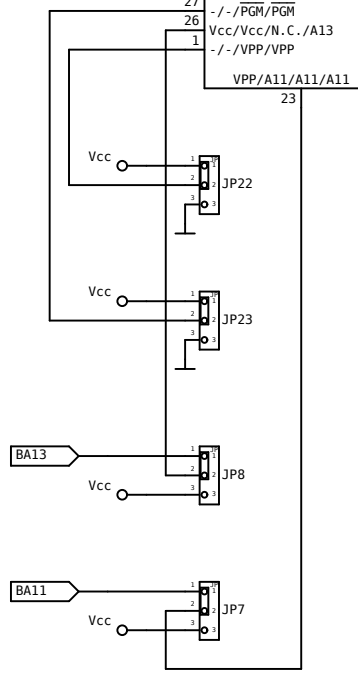
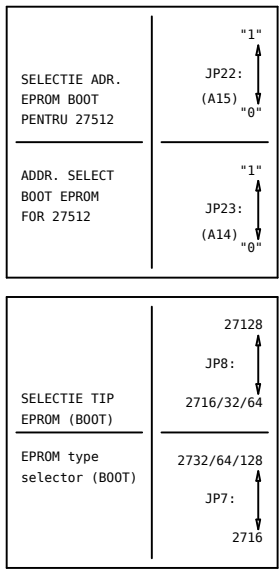


\* (3) JP22 si JP23 dau posibilitatea folosirii unui 27512 ca EPROM BOOT cu selectia uneia din cele 4 zone de 16KB ca zona de EPROM BOOT folosita in mod curent.

\* (3) JP22 si JP23 offer the choice of using a 27512 as BOOT EPROM by selecting one 16KB memory area as the BOOT area currently used.

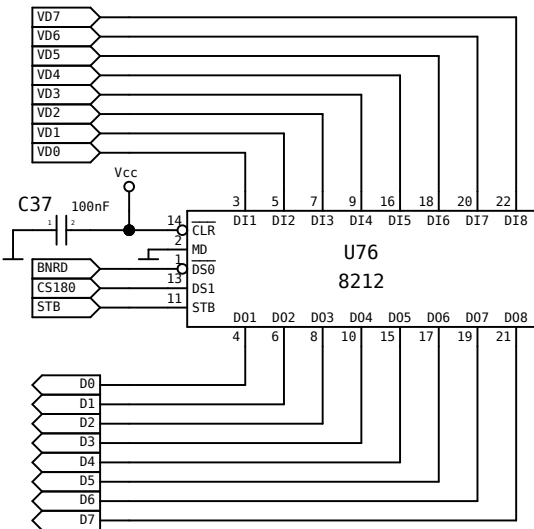
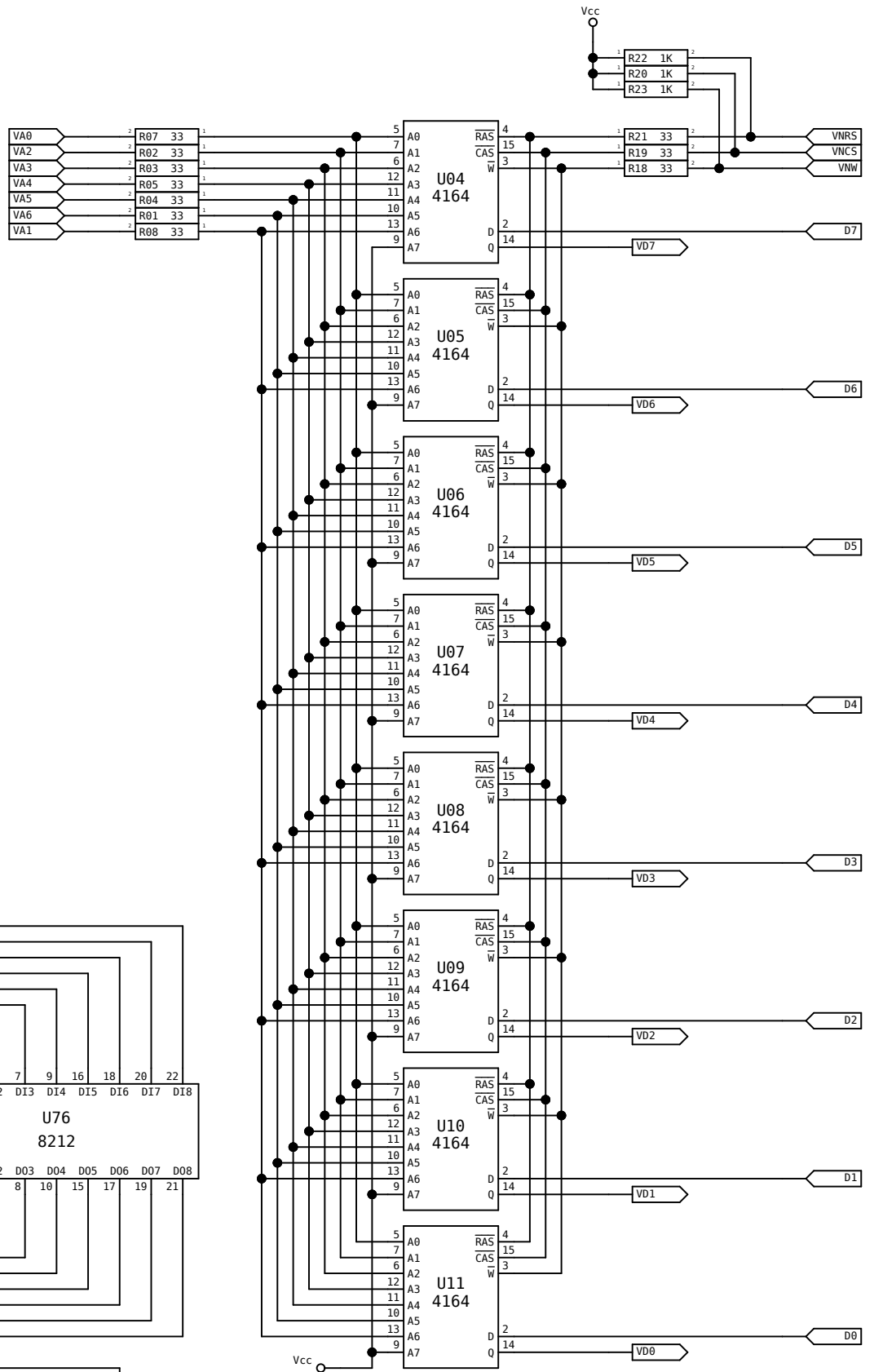
\* (2) JP1 si JP3 folosesc acelasi jumper care este pus la un moment dat ori peste doi din pinii lui JP1, ori peste pinii lui JP3. Atunci cind este pus pe pinii lui JP1, comuta (manual) adresa A15 la "1" sau "0" logic, iar atunci cind este pus pe JP3, adresa A15 a BASIC EPROM este comandata prin software (din BOOT EPROM in configuratia de pornire) cu semnalul T0. Acelasi lucru se intimpla cu JP2 si JP4 si semnalul S0.

\* (2) JP1 and JP3 use the same jumper which at a given moment is either sitting on two of JP1's pins or is sitting on JP3. When seated on JP1, it (manually) switches address line A15 to a "1" or "0" level and when on JP3 the address line A15 of BASIC EPROM is software controlled (by the code in the BOOT EPROM in the startup configuration) with the T0 signal. The same thing happens with JP2 and JP4 and the S0 signal.



	2716	2732	2764	27128	27256	27512
JP7	2-3	1-2	1-2	1-2	1-2	1-2
JP8	2-3	2-3	2-3	1-2	1-2	1-2

TITLE		µC CoBra - Circuitul memoriei nevolatile CoBra µC - Read-only memory circuit	
FILE:	CoBra	REVISION:	3.16a (test, 64/80KB DRAM)
PAGE	10 OF 16	DRAWN BY:	ElectroNNix

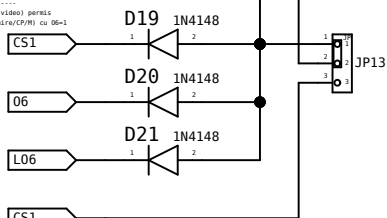


Acest circuit face parte din "Modificarea de 80KB RAM" (adresabili integral).

This circuit is part of the "80K RAM Modification" (fully addressable).

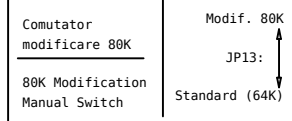
Partea SI cu 3 intrari:

Acces 8212 (citire RAM video) permis doar pentru 106c1 (oprire/OPN) cu 06-1



3-input AND gate:

8212 access (video RAM read) only allowed for 106c1 (startup/OPN) with 06c1



TITLE  $\mu$ C CoBra - Circuitul memoriei video  
CoBra  $\mu$ C - Video memory circuit

FILE: CoBra

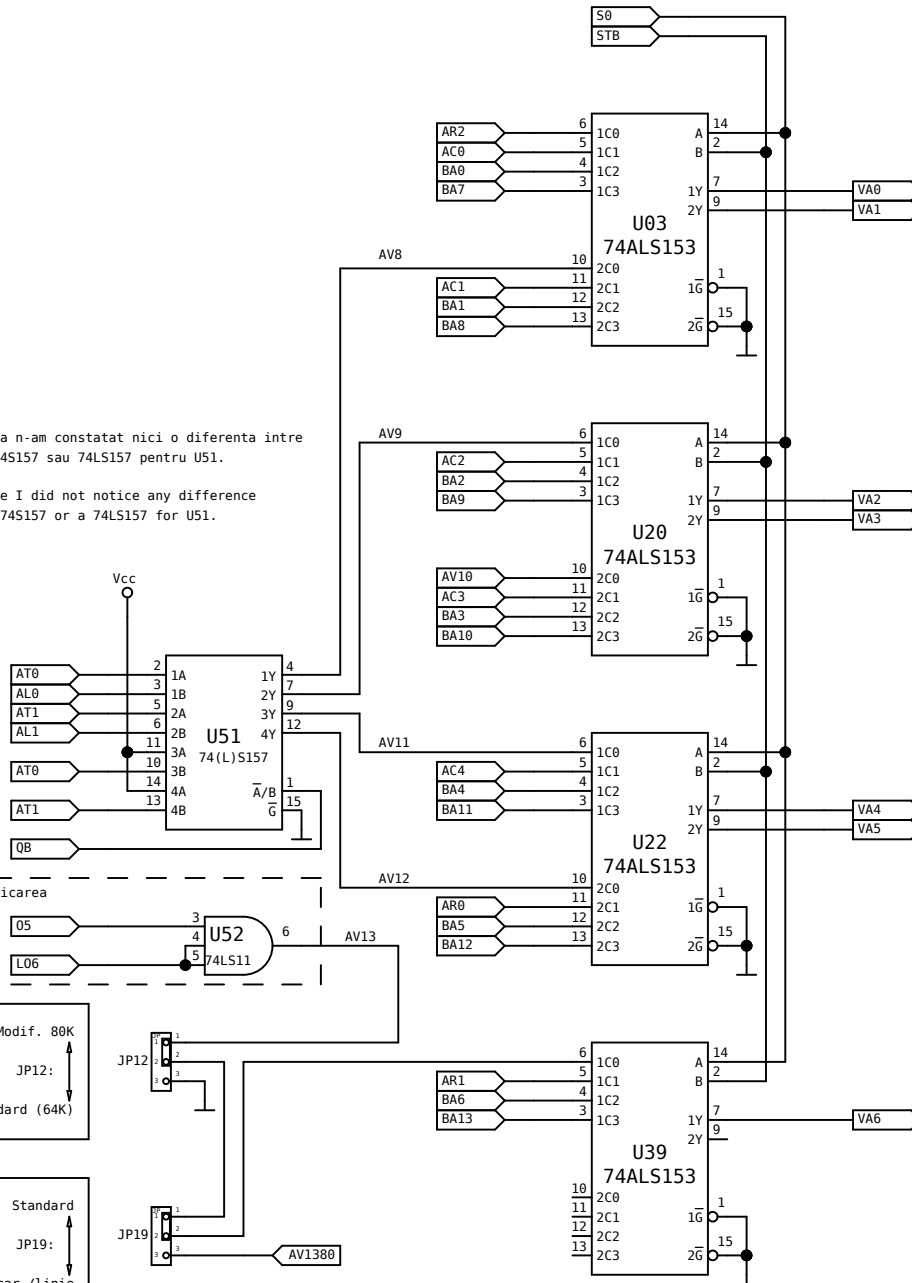
REVISION: 3.16a (test, 64/80KB DRAM)

PAGE 11 OF 16

DRAWN BY: ElectronNix

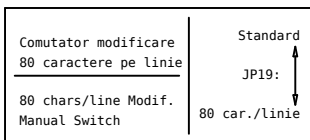
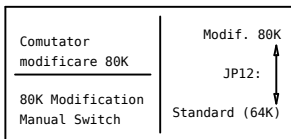
\* (1) In practica n-am constatat nici o diferenta intre folosirea unui 74S157 sau 74LS157 pentru U51.

\* (1) In practice I did not notice any difference between using a 74S157 or a 74LS157 for U51.



Acesata poarta face parte din "Modificarea de 80KB RAM" (adresabili integral).

This gate is part of the "80K RAM Modification" (fully addressable).



\* (2) In practica a fost nevoie sa folosesc 74ALS153 pentru U03, U20, U22, U39 (pentru minimizarea timpului de propagare a adreselor). Cu 74LS153 memoria video NU A FUNCTIONAT CORECT.

\* (2) In practice I had to use 74ALS153 for U03, U20, U22, U39 (for a minimal propagation time of addresses). When using 74LS153 the video memory DID NOT OPERATE CORRECTLY.

TITLE  $\mu$ C CoBra - Circuitul de multiplexare adrese video  
CoBra  $\mu$ C - Video address multiplexer circuit

FILE: CoBra

REVISION: 3.16a (test, 64/80KB DRAM)

PAGE 12 OF 16

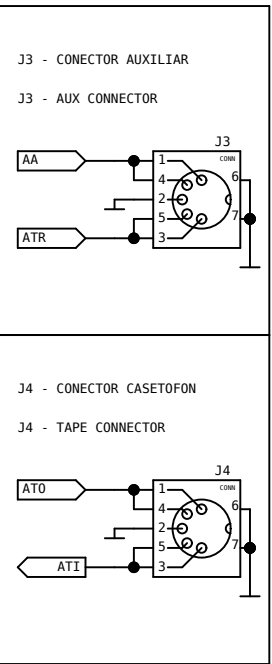
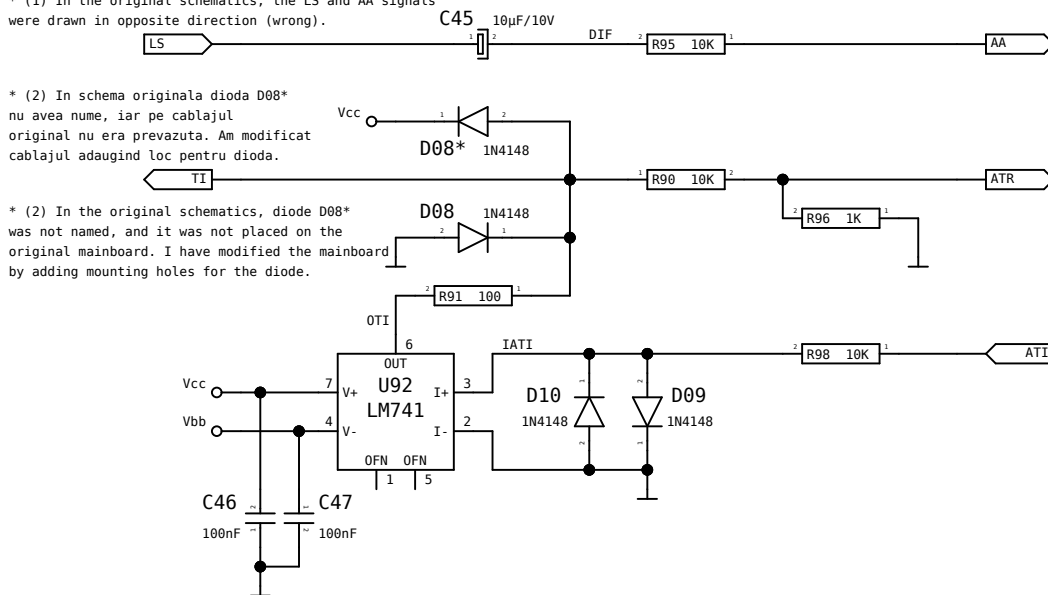
DRAWN BY: ElectronNix

\* (1) In schema originala semnalele LS si AA erau desenate in sens opus (gresit).

\* (1) In the original schematics, the LS and AA signals were drawn in opposite direction (wrong).

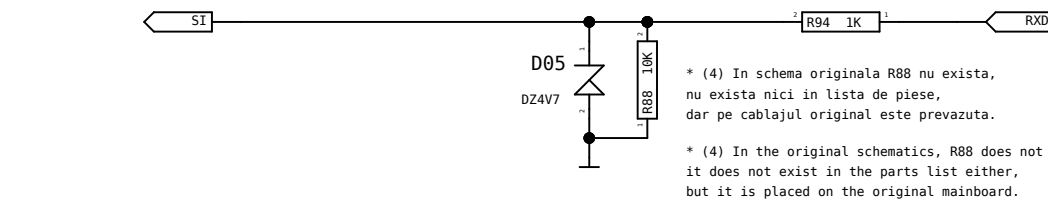
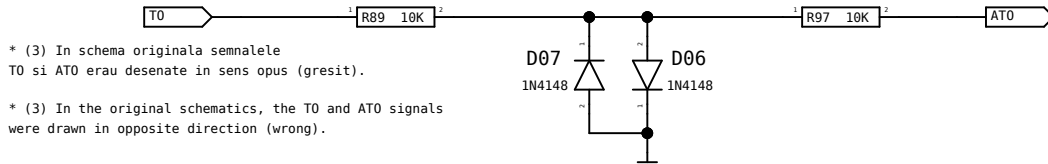
\* (2) In schema originala dioda D08\* nu avea nume, iar pe cablajul original nu era prevazuta. Am modificat cablajul adaugind loc pentru dioda.

\* (2) In the original schematics, diode D08\* was not named, and it was not placed on the original mainboard. I have modified the mainboard by adding mounting holes for the diode.

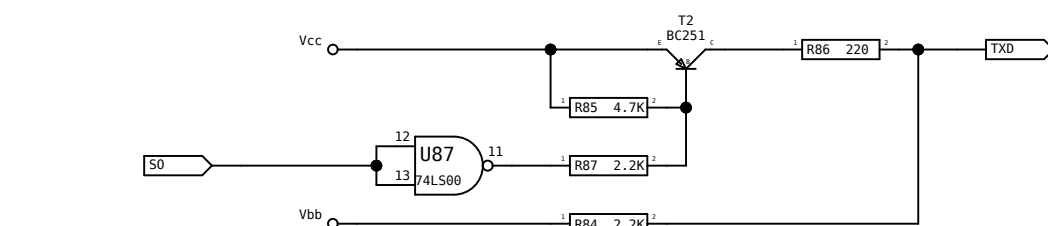


\* (3) In schema originala semnalele T0 si ATO erau desenate in sens opus (gresit).

\* (3) In the original schematics, the T0 and ATO signals were drawn in opposite direction (wrong).



\* (4) In schema originala R88 nu exista, nu exista nici in lista de piese, dar pe cablajul original este prevazuta.  
 \* (4) In the original schematics, R88 does not exist, it does not exist in the parts list either, but it is placed on the original mainboard.

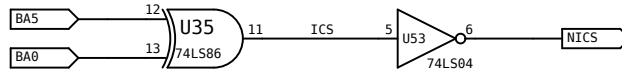


\* (5) Pe cablajul original, poarta U87/13,12,11 era intercalata ca inversor intre U85/12 si U86/11, inversind semnalul I de la U85 la U86 (gresit). Am modificat deci cablajul conform acestei scheme (originale, corecte). (Vezi taieturile #1 si #2 de pe fata 1, #20 si #24 de pe fata 2, si legaturile #18, #20 si #21 de pe fata 2).

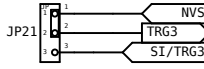
\* (5) On the original PCB, gate U87/13,12,11 was placed as inverter between U85/12 and U86/11, inverting the signal I from U85 to U86 (wrong). I have therefore changed the mainboard layout according to the original (correct) schematic (shown here). (See cuts #1 & #2 on side 1, #20 & #24 on side 2, and rewirings #18, #20 & #21 on side 2).

TITLE		µC CoBra - Circuite de adaptare nivel CoBra µC - Voltage-level adapter circuits	
FILE:	CoBra	REVISION:	3.16a (test, 64/80KB DRAM)
PAGE	13 OF 16	DRAWN BY:	ElectroNNix

\* (1) Pe cablajul original JEXA/8 este legat in mod gresit la BA7.  
De asemenea, manualul original avea JEXA/8 listat ca fiind legat la BA7. Am modificat deci cablajul si schema de fata legind JEXA/8 la BA1 (corect).  
(Vezi taietura #11 fata 1, legatura #22 fata 2)

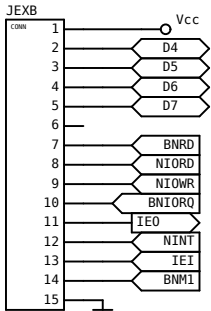
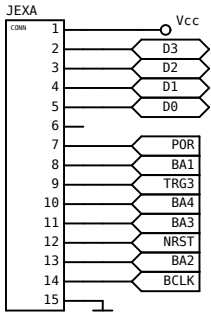


\* (1) On the original mainboard, JEXA/8 was connected (the wrong way) to BA7. Also the original hardware manual had JEXA/8 listed as being connected to BA7.  
I have therefore changed the mainboard layout and this schematic by connecting JEXA/8 to BA1 (correctly).  
(See cut #11 side 1, rewiring #22 side 2)



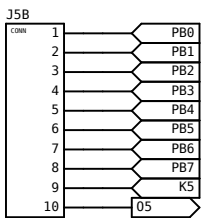
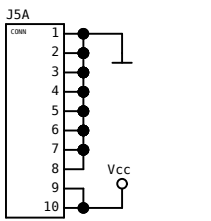
**JEXA+B - CONECTOR INTERFATA FLOPPY DISK**

**JEXA+B - FLOPPY DISK INTERFACE CONNECTOR**



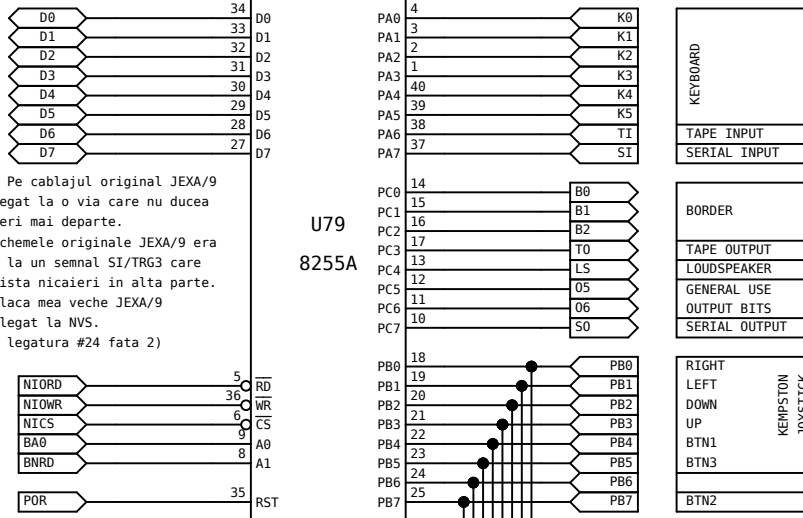
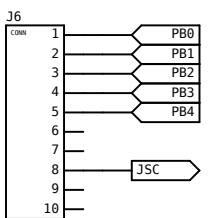
**J5A+B - CONECTOR PORT INTRARE PE 8 BITI ADRESA 0DFH**

**J5A+B - 8-BIT INPUT PORT 0DFH CONNECTOR**



**J6 - CONECTOR JOYSTICK KEMPSTON**

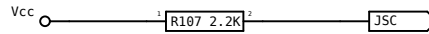
**J6 - KEMPSTON JOYSTICK CONNECTOR**



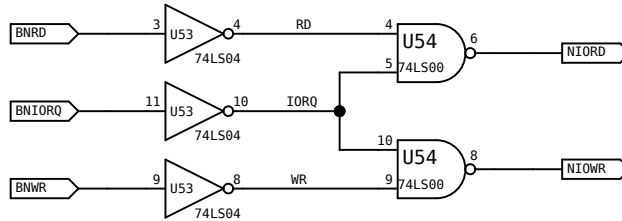
\* (2) Pe cablajul original JEXA/9 era legat la o via care nu ducea nicaieri mai departe.  
In schemele originale JEXA/9 era legat la un semnal SI/TRG3 care nu exista nicaieri in alta parte.  
Pe placa mea veche JEXA/9 este legat la NVS.  
(Vezi legatura #24 fata 2)

\* (2) On the original mainboard, JEXA/9 was connected to a via which was not further leading anywhere.  
In the original schematics, JEXA/9 was connected to a signal "SI/TRG3" which did not exist anywhere else.  
On my old mainboard, JEXA/9 is connected to NVS.  
(See rewiring #24 side 2)

\* (3) Pe cablajul original, R107 este legata in mod gresit la GND in loc de VCC.  
(Vezi taietura #13 fata 1, legatura #19 fata 2)

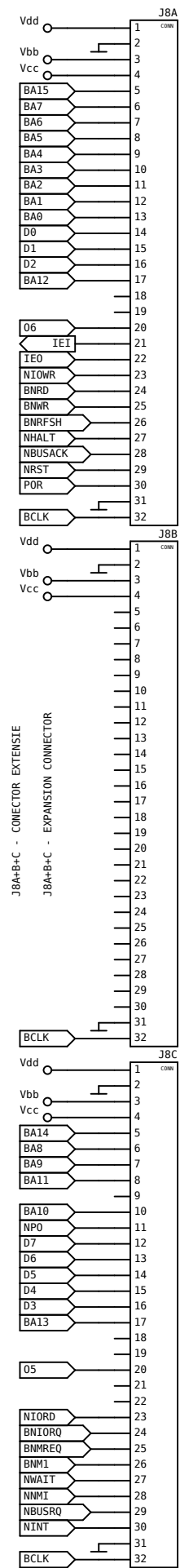


\* (3) On the original mainboard, R107 is wrongfully connected to GND instead of VCC.  
(See cut #13 side 1, rewiring #19 side 2)

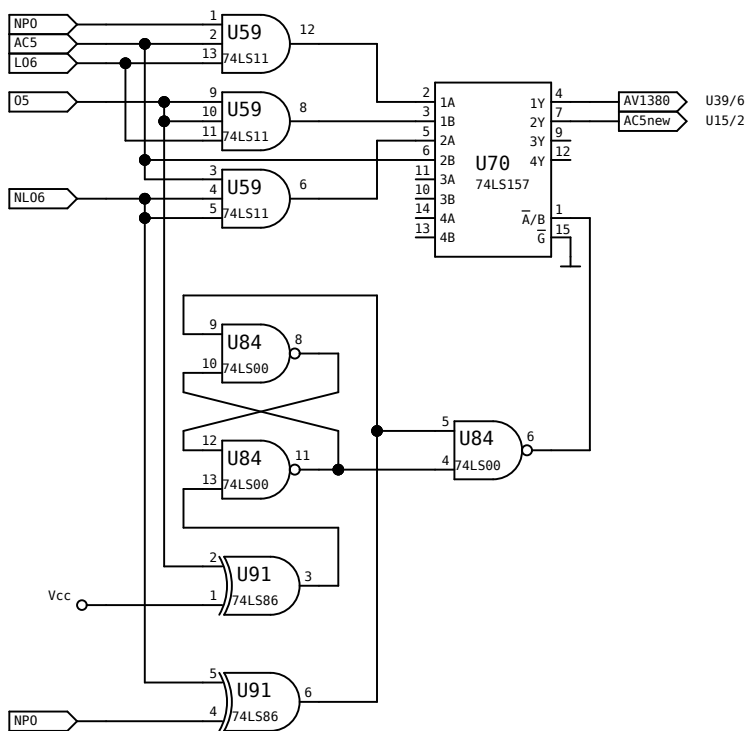


\* (4) Cablajul original avea JSC conectat la J6/pin10 dar manualul original avea JSC listat la J6/pin8. Am schimbat cablajul placii de baza pentru a corespunde manualului.  
(Vezi taietura #5 fata 1, legatura #1 fata 1)

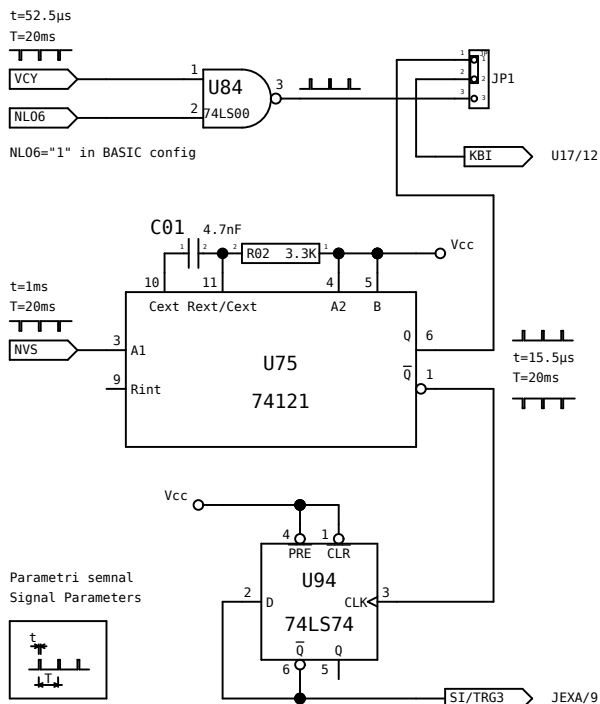
\* (4) The original mainboard had JSC connected to J6/pin10 but the original manual had JSC listed at J6/pin8. I changed the mainboard layout to match the original manual.  
(See cut #5 side 1, rewiring #1 side 1)



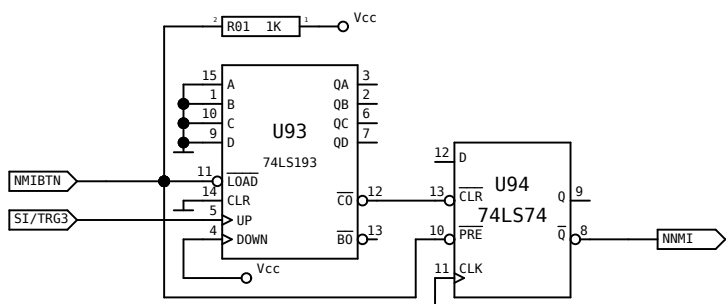
TITLE		µC CoBra - Interfete CoBra µC - Interfaces	
FILE:	CoBra	REVISION:	3.16a (test, 64/80KB DRAM)
PAGE	14 OF 16	DRAWN BY:	ElectroNnix



Circuit modificare 80 caractere pe linie  
80 characters per line modification circuit



Circuit generator intreruperi  
Interrupt generator circuit

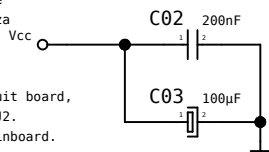


Circuit generator semnal NMI  
NMI generator circuit

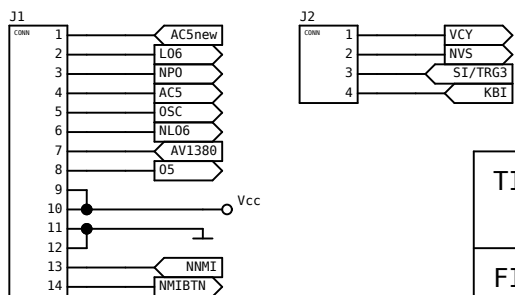
\* (2) Circuitul de mai sus (generator intreruperi), furnizeaza semnalul de intrerupere cu perioada de 20 ms specific Spectrum (KBI) care este mai departe aplicat intrarii U17/12 (7400) de pe placa de baza.  
Din JP1 se poate alege pentru KBI fie solutia din schema originala (VCY x L06), fie semnalul generat la U75/6.  
NOTA: Cablajul imprimat original avea intrarea U17/12 legata la intrarea U17/5, care intrare era legata la semnalul VLD. Deci versiunea originala folosea semnalul VLD ca semnal de intreruperi Basic Spectrum.  
Versiunea 0.2 de placa de baza cu care functioneaza modulul prezentat aici are prevazut un jumper (JP20), din care se poate alege ca semnal de intreruperi Spectrum fie VLD (de pe placa de baza) fie KBI (generat aici).

Acest circuit mai furnizeaza si intreruperile pentru interfata de floppy disk (semnalul SI/TRG3) care este aplicat pe placa de baza la pinul 9 al conectorului de interfata floppy (JEXA/9).  
NOTA: Cablajul imprimat original al placii de baza avea JEXA/9 neconectat, datorita unui traseu lipsa pe cablajul placii de baza, ceea ce nu permitea functionarea interfetei de disc. Placa mea de baza veche (verde) avea JEXA/9 conectat la NVS, iar cea gri avea JEXA/9 conectat la semnalul SI/TRG3 generat ca mai sus.  
Versiunea de placa de baza cu care modulul prezentat pe aceasta pagina functioneaza are prevazut un jumper, din care se poate alege ca semnal de intreruperi pentru interfata floppy fie NVS fie SI/TRG3 (generat aici).

\* (1) Circuitele de pe aceasta pagina se afla pe o placa de circuit imprimat separata, care se cupleaza la placa de baza prin conectorii J1 si J2.  
J1/J2 se infig in conectorii J12/J13 de pe placa de baza.  
\* (1) Circuits on this page are located on a separate circuit board, which is connected to the mainboard through connectors J1/J2.  
J1/J2 are to be inserted into connectors J12/J13 on the mainboard.



J1, J2 - Conectori modul modificari  
J1, J2 - Modif. module connectors



TITLE Modulul cu circuite de modificari  
Modifications module

FILE: CoBra

REVISION: 0.4

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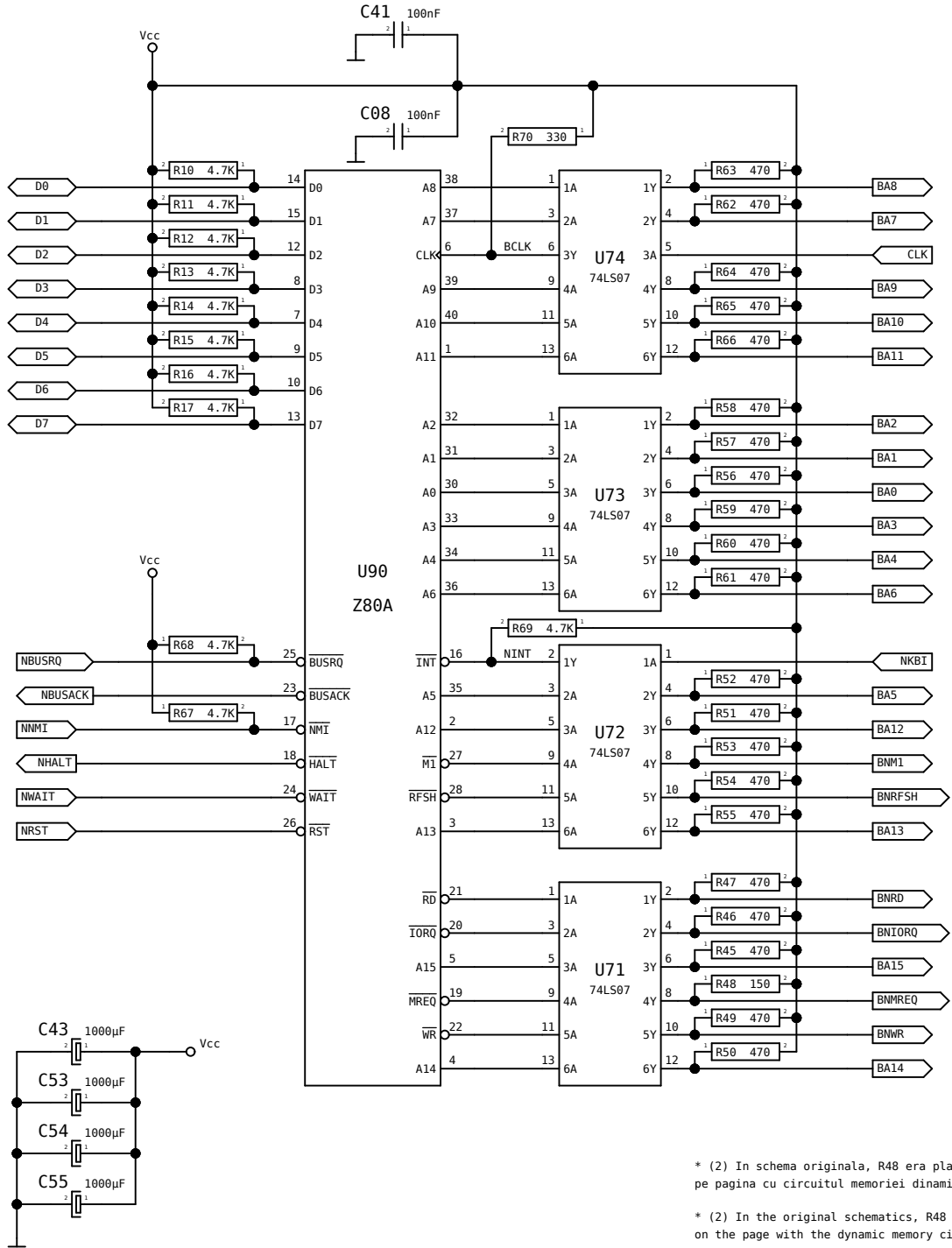
DRAWN BY: ElectronNix

\* (2) In practica am folosit rezistente de 470 Ohm in loc de 680 Ohm, pentru a obtine niste semnale de adrese de putere ceva mai mare.

\* (2) In practice I used 470 Ohm resistors instead of 680 Ohm, in order to have a little more powerful address line signals.

\* (1) In schema originala, U74/6 era legat (gresit) la U90/24, dar corect este ca U90/24 sa fie legat la NWAIT, U74/6 (BCLK) sa fie legat la U90/6 (CLK procesor) si U74/5 sa fie legat la CLK.

\* (1) In the original schematics, U74/6 was connected (wrong) to U90/24, but correct is for U90/24 to be connected to NWAIT, for U74/6 (BCLK) to be connected to U90/6 (CPU clock) and for U74/5 to be connected to CLK.

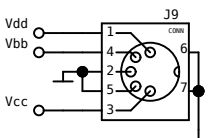


\* (2) In schema originala, R48 era plasata pe pagina cu circuitul memoriei dinamice.

\* (2) In the original schematics, R48 was drawn on the page with the dynamic memory circuit.

J9 - CONECTOR ALIMENTARE

J9 - POWER CONNECTOR



TITLE  $\mu$ C CoBra - Unitatea centrala  
CoBra  $\mu$ C - Central Processing Unit

FILE: CoBra

REVISION: 3.16a (test, 64/80KB DRAM)

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